RESULTS REPORT

2021-11-04 – F5

Abstract

Fabrication run five (F5)

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Summary

Our first instance of a successful JJ curve in fabrication run 3 (F3) had a soft transition and no true superconducting region. We suspected that the JJs in F3 were too large to have coherent tunneling and thus a non-ideal JJ response. Remedially, we shrunk the JJs to the micron scale, near to the reproducibility limit of photolithography in the Waterloo cleanroom. As a result, we have greatly improved our JJ characteristics.

Introduction

Objectives

Our primary objectives of F5 are listed below.

F5:

1. Improve JJ I-V characteristic
    a. Reduce JJ size to the limit of UV photolithography
    b. Increase scaling factor between JJs and collector JJ
    c. Reduce distance between JJs and collector JJ
    d. Isolate bottom electrodes
    e. Rely on PBCO layer to insulate metal contact traces
2. Improve fabrication process
    a. Dose tests
    b. Contacts improvements

Design

In this iteration we continue to rely on the series JJ structure depicted in "Current Design" below where the JJ being tested is labeled "JJ" and the "Collector" acts as a short to the bottom electrode. PBCO is intentionally left on the bottom electrode to protect it from ion mill damage. To our advantage, the PBCO also acts as insulating layer allowing us to deposit metal contact traces that connect wirebonding pads to the JJs (see Figure 2 below), which is critical to shrinking the devices.

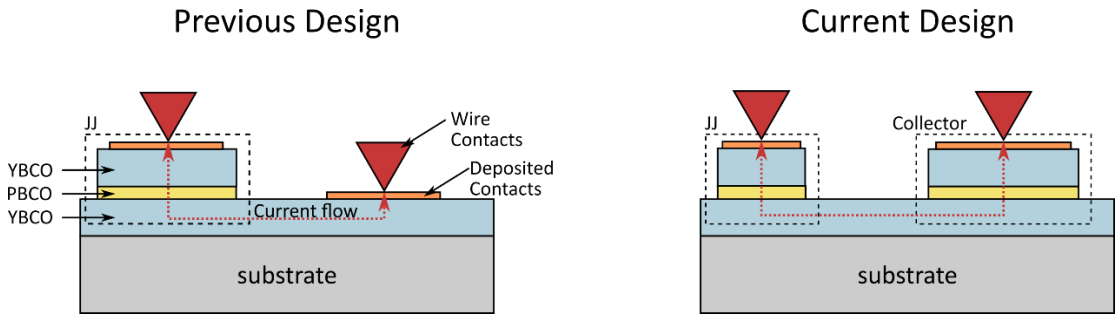

Figure 1: Present and previous designs showing the path of current flow

Major changes were made to the photolithography pattern to accommodate our objectives. JJs were shrunk as small as 2 µm x 10 µm, which is over **6,000 times smaller than F3**, with scaling factors between 5 and 20, and the distance between the JJ and its collector is over 200 times smaller than F3. Below is the new photolithography pattern for F5, shown from the top down. The JJs and collector are in orange, while

the surrounding black/blue is YBCO that is etched down to the PBCO layer. Yellow is the metal contact traces which connect the very large wirebonding pads (not shown) to the very small JJs.

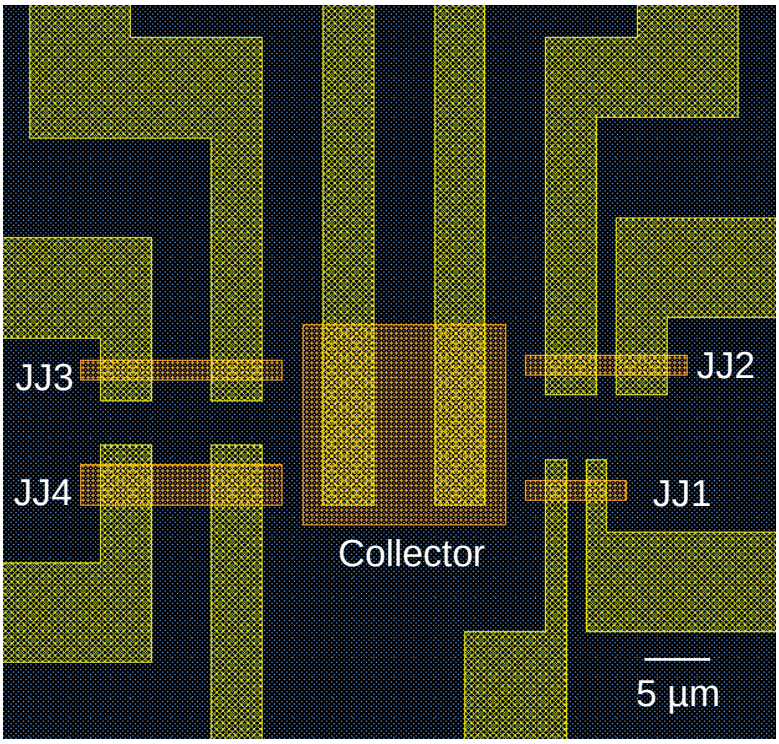

Figure 2: Photolithography design showing our four JJs surrounding the collector junction

The smallest junctions we could reproducibly create with UV photolithography in Waterloo is ~1 µm x 1 µm, which gives a theoretical maximum density of **250,000 JJs/mm^2**, if we remove the collector. Compared to D-Wave (1,030,000 JJs on an 8.4mm^2 chip = **122,000 JJs/mm^2**) and TSMC (**150 million transistors/mm^2**) we are already projected to be competitive. Of course, this is just a rough estimate because D-Wave and TSMC chips have real circuits with elements other than JJs and transistors that take up additional space. We could later investigate a realistic density by creating a small JJ-based circuit and extrapolating its maximum density on a chip. Furthermore, TSMC has access to extreme UV photolithography, which can pattern devices down to ~ 50 nm x 50 nm. This is a distinct advantage in terms of device density and while we do not have access to EUV technology in Waterloo, we do have electron-beam lithography (EBL). EBL can easily pattern 50nm x 50nm devices, which would give us a theoretical maximum density of **100 million JJs/mm^2**. EBL is not typically used in industry because it is much slower than EUV, but it could still help us define our range of possibility in JJ size. It should be noted that there **will** be limitations other than the lithography tool that may not allow us to get near 50nm (Ic, etching profile, etc), however, 50nm – 250nm is a good initial target (D-Waves LTS JJs are 250nm x 250nm). Finally, our material is also unique in its ability to be stackable, which will significantly increase JJ count, without taking any additional space on the chip. It is relatively straightforward for us to stack JJs on top of each other when series JJs are required while LTS and c-axis HTS JJs struggle to be stackable.

Results

Tc

Tc for the top YBCO layer has improved since F3 with fabrication optimizations and is now the same as we originally measured in Cornell. The resistance at temperatures above Tc has also decreased, which is indicative of our improved metal contacts. The resistance is zero when the temperature is about 72K.

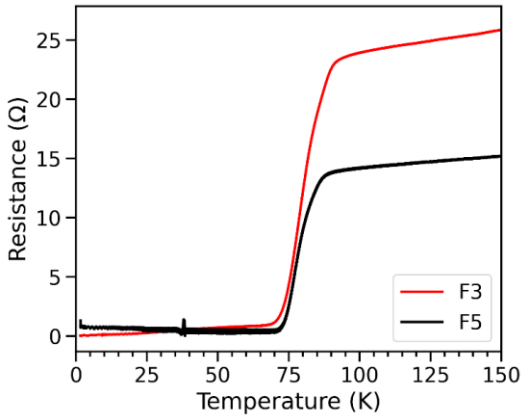

Figure 3: Tc for the top YBCO layers in F3 and F5

I-V

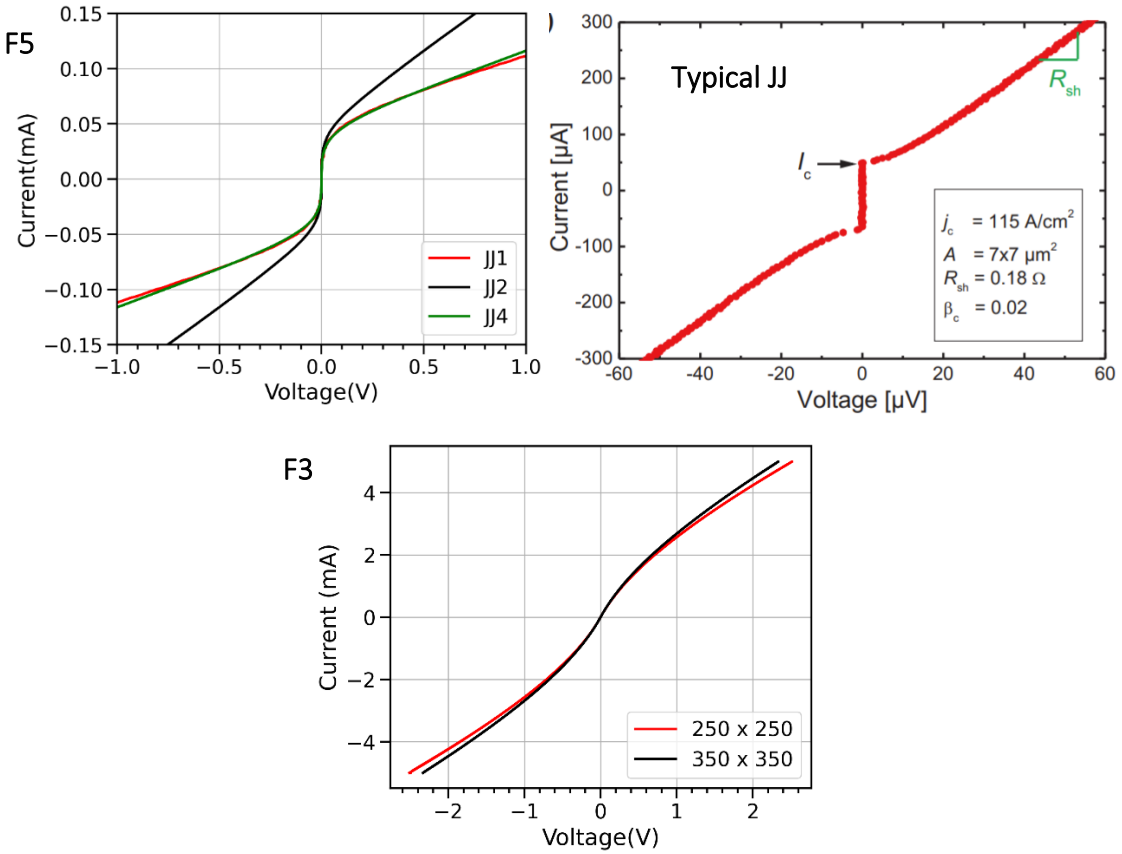

Figure 4: JJ I-V plots for F5, a typical JJ, and F3 for comparison. All are at 2K.

An I-V plot of the F5 JJs is shown above with a typical JJ and the plot of F3 JJs for reference. Notice how similar the shape of the F5 curve is to a typical LTS/HTS junction, especially in contrast to the results in F3. The JJs in F5 show a true superconducting state, while F3 gave us a first hint at a JJ response. We can say roughly that F5 JJs can support **100 times more supercurrent** and they have **180 times lower (normalized) resistance** than F3.

If we compare our F5 JJs to other HTS JJs in Table 1 below, we find similar critical current densities although we have a large resistance that may be obscuring some of our current (see the rounded part of the I-V plot in F5 above). The typical JJ plot has a sharper corner instead of a curve at the critical current (Ic). Critical current is the maximum amount of supercurrent that can flow through the JJ before it becomes resistive and critical current density (Jc) is the critical current divided by the size of the JJ. Jc allows for direct comparison of differently sized JJs.

The large resistance also makes it impossible to state an accurate IcRn product. The IcRn for F3 and F5 shown in Table 1 is very rough since they were calculated using R_{sh} and R_{sh} completely masks Rn in our data. IcRn is an important JJ characteristic that defines the junction frequency, which affects many of our JJ applications (RSFQ, JPU clock cycles, etc.). Higher IcRn produces a higher frequency JJ according to $f_c \equiv \frac{2e}{h} I_c R_N$. IcRn also affects the noise levels in a SQUID and ultimately determines the sensitivity of the sensor. Higher IcRn produces lower background noise and higher sensitivity. The FIB JJ/SQUID project

should improve resistance and allow us to state a more accurate IcRn for our devices. With some tuning, we expect Rn to be >10Ω and IcRn to be >200 μV. For reference, a JJ with IcRn > 2000 μV will have a characteristic frequency >1THz[1].

Table 1: Summary of our JJ characteristics compared to literature.

Source	Critical current density (A/cm^2)	R_{sh}/Rn (Ω)	IcRn (μV)	JJ area (μm x μm)	I-V curve type	Insulator type	Insulator thickness (nm)	YBCO type
F3	1.8*	650	$7.3x10^5$	250 x 250	Overdamped	PBCO	8	a-axis
F5-JJ1	150	17.5K	$3.1x10^5$	2 x 6	Overdamped	PBCO	8	a-axis
[2]	110	5.7	160	5 x 5	Underdamped	PBCO	10	c-axis
[3]	170	9.4	400	5 x 5	Underdamped	PBCO	25	c-axis

* Note, critical current was obscured in F3. This number is very rough

It is also important to have an 'overdamped' JJ for SQUID applications. During an I-V measurement, data is taken forward (from negative to positive) and backward (from positive to negative). If the forward and backward measurements follow the same path, then the JJ is non-hysteretic and overdamped. If they follow different paths, then the JJ is hysteretic and underdamped. Overdamped junctions have negligible capacitance and a McCumber-Stewart parameter (β_c) <<1 while underdamped junctions have significant capacitance and β_c >>1. Overdamped junctions are important in SQUID design for response symmetry and sensitivity. We have an overdamped junction unlike many devices that are reported in literature.

Temperature Study

We can begin to understand some operational parameters of the JJ by completing a temperature study. A temperature study tells us about the temperature limit for the JJ. The plot below shows the temperature data for JJ1 in F5, with each line representing a different temperature for the same JJ. Like F3, we have lost the characteristic JJ shape by 20K. We are likely seeing the effects of a bad Tc of the bottom YBCO layer, since we know the top YBCO layer is very superconducting until 70K. However, we expected the temperature characteristics of F5 to remain the same as F3 because the major fabrication steps (ion mill, baking, cleaning) are identical. The next iteration will focus on improving the bottom electrode.

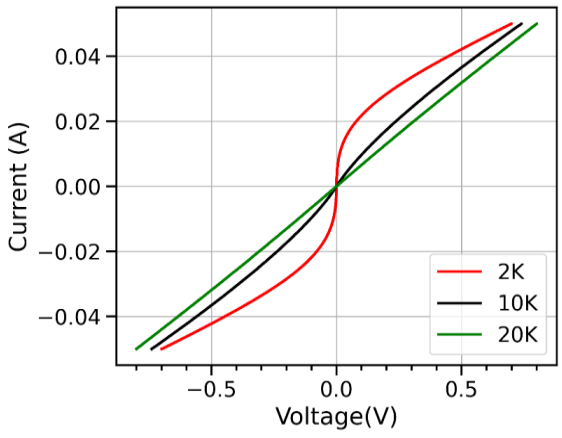

Figure 5: I-V plots of JJ1 at three different temperatures

Conclusions and Next Steps

We have demonstrated significant improvement over our first a-axis trilayer JJ. F5 JJs have 100 times better critical current density than the previous iteration and will be usable for our applications once we correct the large resistance. The FIB JJ/SQUID project will provide significant information on how to improve the bottom YBCO, possibly showing further improvements over F5. Below is a list of key elements to improve in the next iteration (after the FIB project) and how they might be achieved.

1. Improve Tc of the bottom electrode
    a. Reduce temperature of heated steps
    b. Reduce ion mill depth
    c. Reduce ion mill power
2. Improve IcRn by increasing Ic
    a. Add a true insulating layer (SiO2, etc) instead of relying on our thin PBCO layer to insulate the contacts
    b. Reduce thickness of PBCO
    c. Reduce resistance in the device as stated in 1.

For completeness I have listed the major differences between F5 and F3 and key elements of the next design.

Table 2: Key elements for each fabrication run

Previous Design (F3)	Current Design (F5)	Next Design
• Etch only to the PBCO layer • Ion mill angled etch • Contacts with excellent adhesion (Ti/Au, Au wires) • One continuous bottom layer	• Etch only to the PBCO layer • Ion mill angled etch • Increase contact complexity • Isolated bottom layers • JJ size on micron scale • Increased scaling factor • Reduced distance between JJs	• Reduce ion mill etch depth • Ion mill angled etch • Add insulating layer for improved contacts • Isolated bottom layers • JJ size on micron scale • Increased scaling factor • Reduced distance between JJs • Reduce temperature of heated steps

Appendix

Scaling with Junction Area

There are a few results that require further investigation. Primarily, the relationship between I-V plots and their junction area remains unexplained. In an ideal set of junctions, Ic and R_{sh} should scale with junction area, and plots of current density should overlap (i.e. Jc and IcRn should be material constants). However, we can see in the plots below that JJ1 and JJ4 overlap before normalization and none of the curves overlap after normalization. If the curve for JJ2 is scaled by 0.77 then Ic of JJ1 and JJ2 overlap but R_{sh} (α 1/slope) is still drastically different. Our results suggest that the effective junction area is different than the designed junction area or, if the data is being dominated by a series resistance, the path of current flowing through JJ1 to the collector has the same resistance as JJ4 to the collector, while the path for JJ2 is almost half as resistive.

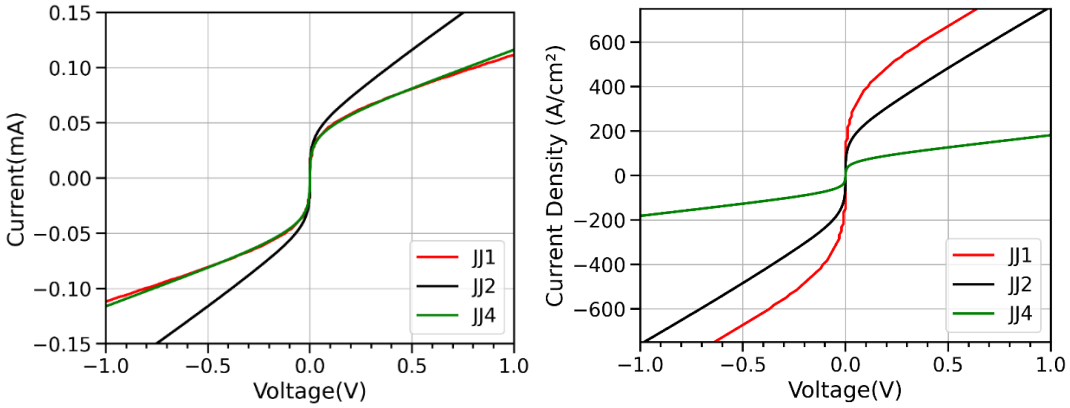

Figure 6: Current and Current density vs voltage for each JJ

We can investigate other current paths by using the other JJs as collectors for JJ1 (Figure 7 below). First, you can see that the I-V plot of JJ1-original (with regular collector) has deteriorated over time. JJ1-repeat is the same measurement as JJ1-original with some additional time exposed to air. This is good evidence that we need to start encapsulating our devices. Second, the resistance decreases (slope increases) when the smaller JJs are used as a collector. The choice of collector should not greatly affect the I-V curve if the collector is larger than the JJ being tested. Two differently sized JJs in series might show a second superconducting transition but, in our data, we see clear changes in resistance with different collectors and no second transition. In fact, the two smallest collectors (JJ1-JJ2 and JJ1-JJ4) show the smallest resistance while the large collector has 4x larger resistance. We could be seeing:

- Resistance in the bottom electrode, however, resistance does not scale according to separation between JJs
- Resistance in the top electrode. The collector has a relatively large unprotected top electrode that may be introducing a lot of resistance.
- Other, unknown issue with the collector

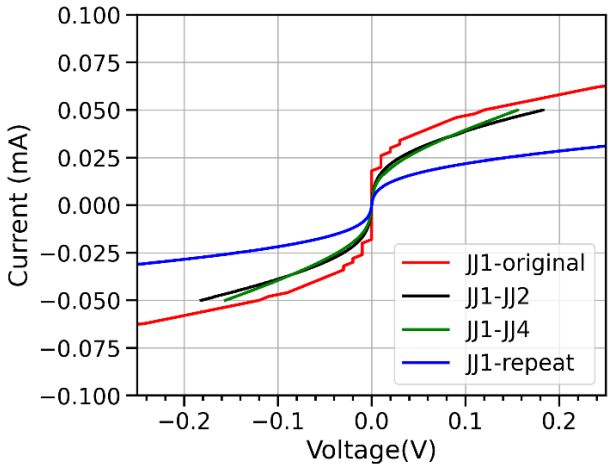

Figure 7: I-V for JJ1 using other JJs as the collector

2-pt Contacts

Finally, we can look at JJ5 and JJ6, which were 2-pt contacted JJs and previously unmentioned. We can see that the data is mostly obscured by a resistance without a true Ic. This is because the 2-pt contact method requires very good ohmic contacts, which we are still improving. Ultimately, 2-pt contacts are used to contact real devices, so we will need to continue verifying these types of JJs as we improve contact resistance.

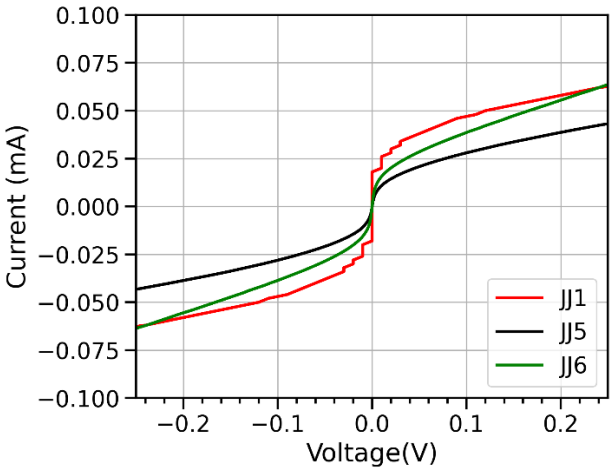

Figure 8: I-V for 2-pt contacted JJs

References

[1] Grossman E N 1994 Terahertz Shapiro Steps in High Temperature SNS Josephson Junctions *IEEE Trans. Microw. Theory Tech.* **42** 707–14

[2] Kuroda K, Wada Y, Takami T and Ozeki T 2003 Fabrication of Full High-Tc Superconducting YBa 2Cu3O7-x Trilayer Junctions Using a Polishing Technique *Japanese J. Appl. Physics, Part 2 Lett.* **42** 7–10

[3] Fujimoto E, Sato H, Yamada T and Akoh H 2002 All YBa 2 Cu 3 O 7-δ trilayer junctions with YBa 2 Cu 3 O 7-δ wiring layers *Appl. Phys. Lett.* **80** 3985–7