Investor Presentation

August 12, 2021

Ambature, Inc.

Presented by CEO Ron Kelly

AMBATURE

Ambature, Inc. designs superconducting quantum materials to power an innovative and sustainable future.

Presentation Outline

- Intellectual Property
- Commercial & Military Use Cases
- Go-To-Market Strategy
- Financial Metrics
- Q&A

Intellectual Property

Intellectual Property

Ambature has the leading global IP portfolio covering **a-axis High Temperature Superconductors (HTS)** with **Extremely Low Resistance (ELR)**—key fundamental technology **enabling next-generation applications** across multiple end markets.

Portfolio Differentiators

- **Insulators vs. Semiconductors vs. Superconductors**
- **ELR materials** combined with **unique a-axis architecture**

Portfolio Focuses

- High-speed/energy-efficient **processing, sensing, imaging**
- **Clean energy** creation, transportation and storage of electricity
- **Higher-temperature superconductors**

200+ Active Patents	3700+ Unique Claims
20+ Product Applications	14+ Years of Research

IP Validation

- Our PCT filing and additional individual patents have issued in **8 of the 10 largest economies in the world.**
- We have one of **the largest superconductivity IP portfolios in the world.**
- **190+ citations** include TSMC, Samsung, Qualcomm, GlobalFoundries, IBM, GE, BOE in China and the Chinese Academy of Sciences.
- **Peer-reviewed Applied Physics Letters published** our Cornell wafer research in February, building upon prior validation from NASA's Jet Propulsion Lab.
- **Our first a-axis Josephson junction (JJ)** was created in June.

Josephson junction Timeline

2018-2019
International PCT filing issues in the US and China

Oct. 2019
Method of making JJ patent issues in the US

Jan. 2019
Cornell a-axis wafer research project begins

Oct. 2020
Cornell publishes their research regarding Ambature's a-axis wafer technology on arXiv.org

Feb. 2021
APL Materials journal publishes the Cornell paper

May 2021
Ambature produces even higher-quality wafers than the ones in the Cornell paper in Ambature's Waterloo facility

June 2021
Ambature files US and international patent protection **for a-axis wafer and integrated c-axis and a-axis technologies**

June 2021
Ambature demonstrated the first a-axis JJ in the Waterloo facility

July 2021
Ambature begins **prototyping** of 20+ use cases for JJs

APL Peer Review Comments

Max Planck Institute

Samples obtain high quality, high superconducting transition temperature ~85 K, phase purity and improved surface quality with rms roughness less than a-axis superconducting coherence length, making these films promising candidates for fabricating Josephson junctions and other electronic devices.

Brookhaven National Lab

This is expected to be beneficial for fabrication of high-Tc Josephson junctions, a technologically very important and yet so far largely elusive target. This paper presents a significant step towards reaching this goal.

Commercial & Military Use Cases

Solving the Semiconductor Industry's Problem

Power

Multidirectional in-plane current flow

Speed

Lower electrical resistance increases compute speed

Efficiency

No/low resistance dramatically **reduces energy loss** in systems

Density

Enables transistors and/or JJs to be packed closer together with less heat

Extremely high-frequency processors

Extremely energy-efficient processors

Small, dense devices without the usual heat constraints

Advantages Along the A-Axis

Unique Growth Orientation

Planes of a-axis YBCO (or other materials) **are grown vertically like walls** rather than horizontally like sheets.

The flow of current in our materials determines the structure of our JJ.

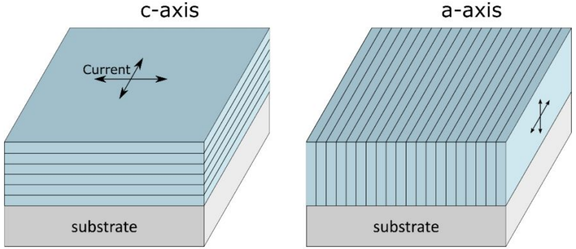


Fig. 1. c-axis and a-axis layers with indicated current flow

Facilitates Tunneling More Efficiently

C-axis devices require more complex circumvention techniques such as the ramp junction illustrated below. A-axis designs seamlessly direct current flow between superconducting layers.

Application Benefits

- **Controlled current** in two directions
- **10X** coherence length
- **Easier mass commercialization fabrication i**n existing semiconductor foundries
- **Tunneling** is optimized in-line with the plane

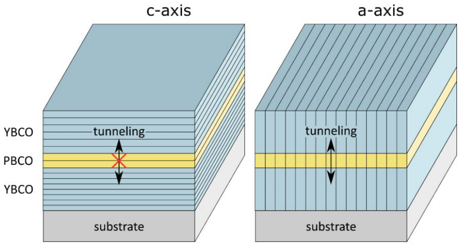


Fig. 2. Stacked c-axis and a-axis YBCO JJs. The orientations of the layers determine if tunneling is possible

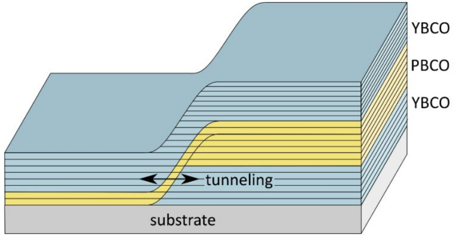
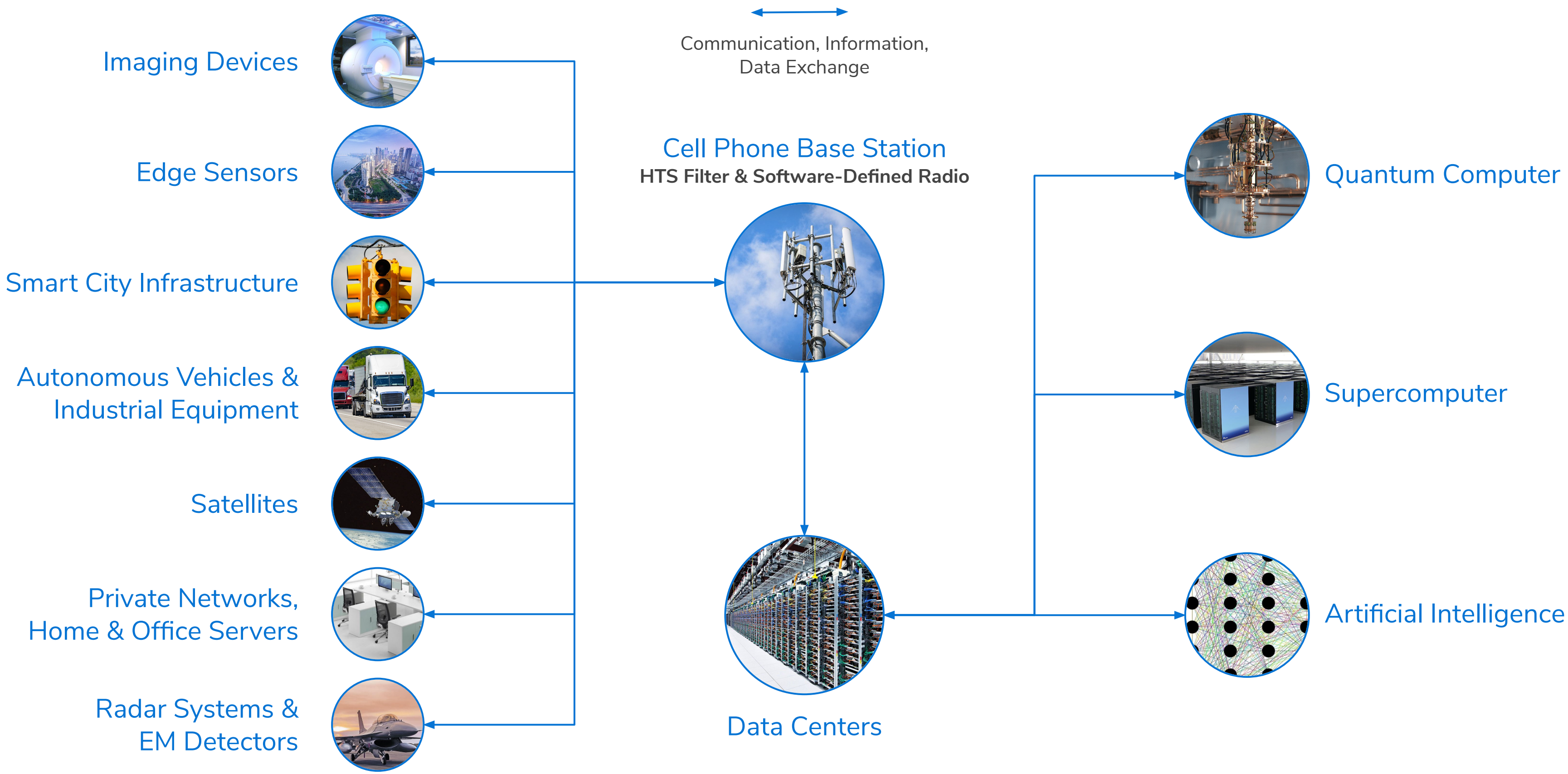


Fig. 3. c-axis ramp junction. Notice how it requires two PBCO layers, one as a thin tunnel layer and the other to isolate in the vertical direction

High-Performance Computing and Sensing



Military & Civilian Infrastructure

Ambature’s sensing capabilities enhance multiple military and civilian applications.

- **Positioning, Navigation and Timing** (PNT) signals need to be enhanced
- PNT signals need to be **continuous and accurate**, even where GPS is not available
- Communications should be **unjammable**

Magnetic Anomaly Navigation

Alternative to GPS

Non-Destructive Testing

Detecting corrosion & cracks

Advanced & Quantum Radar

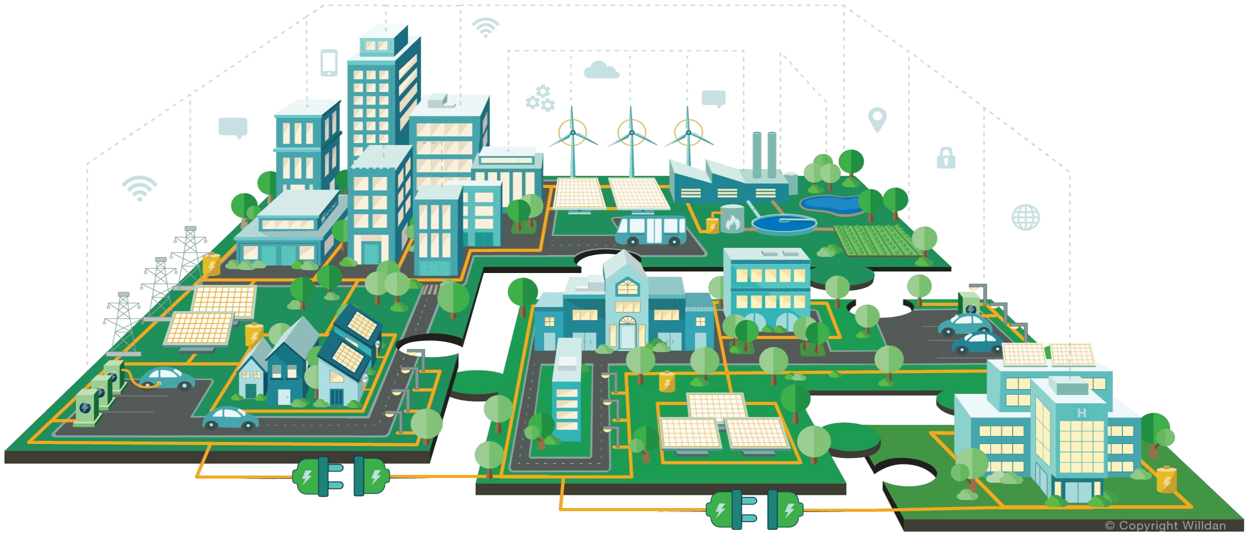
See while not being seen

Bistatic, Over-the-Horizon, Quantum, etc.

Electromagnetic Wave Detection

Infrared Imaging

Clean Energy Infrastructure & ESG



Generation

Rotating Machines (like Motors and Generators)

Transmission

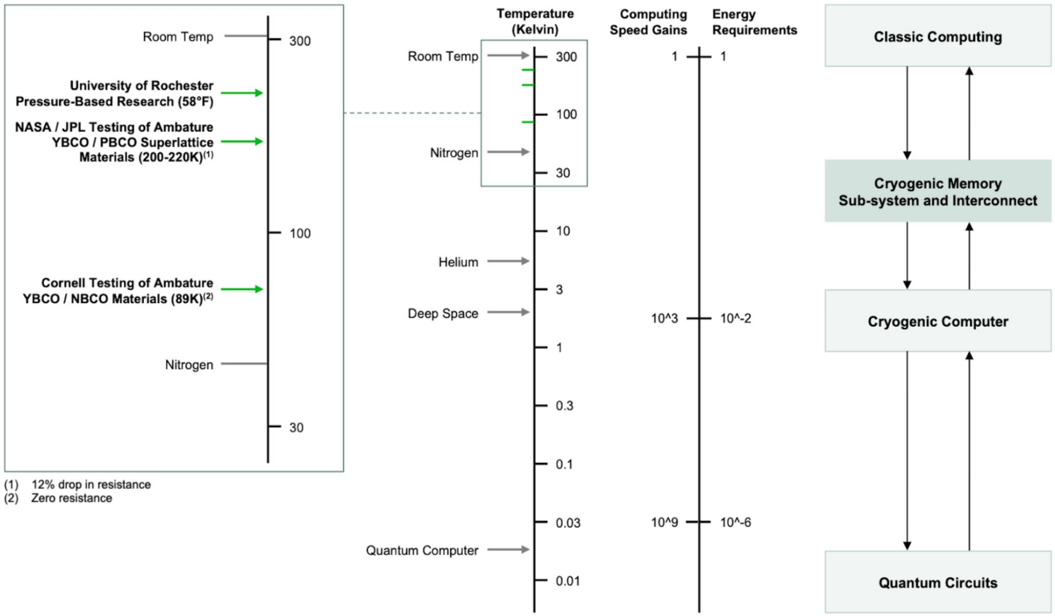
Power Transmission Components, Transformers, Fault Current Limiters, Smart Grids

Storage

Batteries, Energy Storage Devices, Supercapacitors

High-Temperature Superconductors

NASA's Jet Propulsion Lab published that Ambature has **"fabricated and tested a material that arguably holds promises for room temperature superconductivity."** The **Chinese Academy of Sciences endorses a-axis architecture** for China's future superconductivity applications.

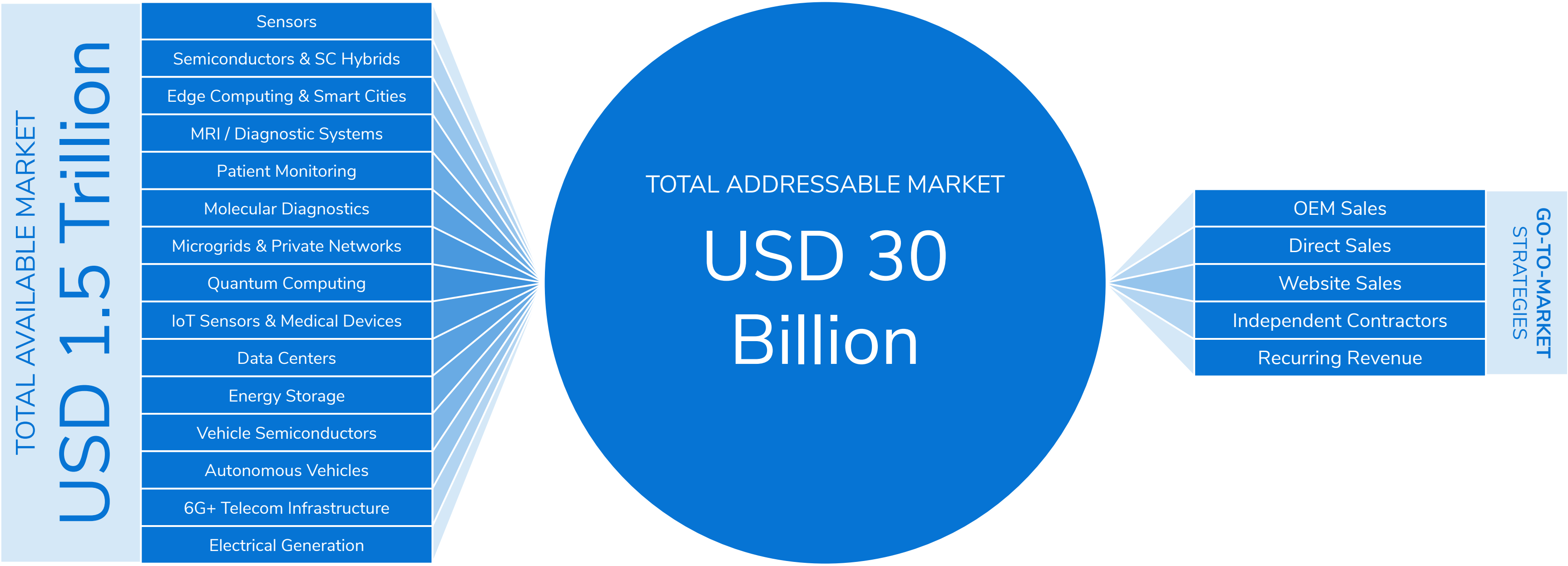


Go-To-Market

Macro Market Drivers

- Increasing need to deal with **resistance/heat issues** by cooling to enhance performance and cost/efficiency
- Proliferation of **autonomy, advanced wireless, cloud servers / data centers, IoT and AI**
- **Growth in all market segments** where we have a use case
- Need for **new materials and architectures** to derive more power, speed, efficiency, density and reliability from silicon wafers
- Smaller/cheaper **cryocoolers** entering the market
- The need for **longer quantum coherence** to drive quantum computing & other use cases
- **Energy efficiency objectives** and **national security concerns** regarding the chip supply chain coming from the Biden Administration and Congress
- **Recent chip shortages** impacting large segments of the economy such as automakers

Market Size


TOTAL AVAILABLE MARKET
USD 1.5 Trillion
Sensors
Semiconductors & SC Hybrids
Edge Computing & Smart Cities
MRI / Diagnostic Systems
Patient Monitoring
Molecular Diagnostics
Microgrids & Private Networks
Quantum Computing
IoT Sensors & Medical Devices
Data Centers
Energy Storage
Vehicle Semiconductors
Autonomous Vehicles
6G+ Telecom Infrastructure
Electrical Generation
TOTAL ADDRESSABLE MARKET
USD 30 Billion
OEM Sales
Direct Sales
Website Sales
Independent Contractors
Recurring Revenue
GO-TO-MARKET
STRATEGIES

Near-Term Technology Roadmap

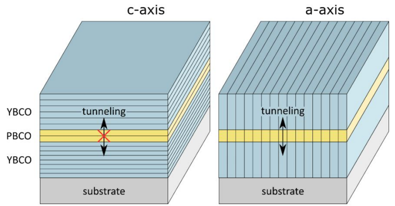
- Develop **prototypes and measure KPIs** for telecoms, data centers, autonomous vehicles, medical devices, and advanced/quantum radar
- Develop **stand-alone JJ processors and sensors** for the Edge & Data Centers
- Further develop the core JJ technology and SQUIDs for **integration with CMOS, silicon, and high-speed interconnects**
- Further develop high-temperature superconductors to **at least -30°C**
- Identify **key foundry partners** for commercial and military applications
- Scale Ambature with **50-80 additional employees**

Key Differentiators & Value Propositions

Ideal Geometries

Ambature has achieved a-axis superconducting wafers with best-in-class thin and smooth layers.

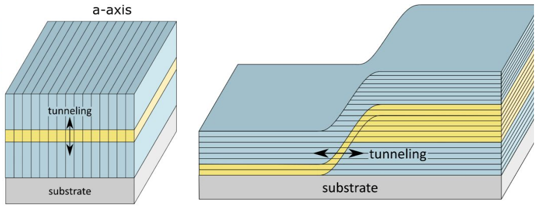
Vertically-aligned devices enable current flow in both horizontal and vertical directions, **allowing direct tunneling of current from one superconductor to the next.**



Simpler Fabrication

A-axis stacked devices allow for easier fabrication **as all layers are grown at once,** speeding up development and **reducing defects.**

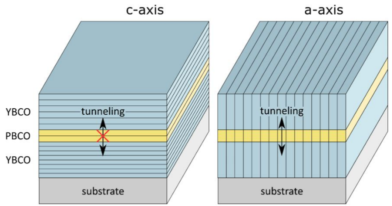
A-axis devices like JJs can be fabricated using **standard semiconductor equipment** in a simplified fabrication process.



Better Superconductors

A-axis stacked devices have perfectly aligned tri-layers, creating an **ideal coherence length and critical current.**

Ambature's materials transition to be superconductive at approximately 90 Kelvin, requiring less cooling than traditional niobium-based JJs.

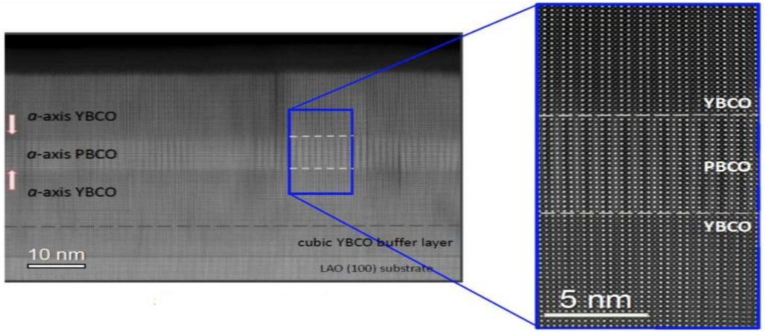


Cornell Delivers World-Class Results

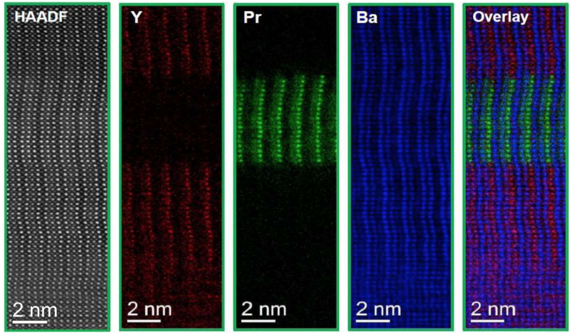
Ambature/Cornell used MBE and a **patented fabrication process** to successfully develop **extremely thin and smooth 100% pure a-axis** superconducting wafers, setting the stage for **commercialization.**

Publication Findings

- The thin and smooth design creates **ideal material for Josephson tunneling and junctions.**
- **Achieved 100% a-axis** YBCO-PBCO-YBCO tri-layer crystal synthesization.
- Demonstrated very thin and smooth **"sharp interfaces"** with the ability to go thinner.
- **Clearly defined interfaces** between tri-layers with a clear a-axis structure.



STEM-HAADF shows high-quality layers with near-perfect atomic alignment at interfaces



STEM-EELS shows precise control of layer composition

Ready for Commercialization

	KPIs & Standard Metrics	Ambature
Commercial Recipe	• Leverage a temperature-ramping procedure during deposition to **produce smooth, a-axis growth** • Transition to superconductivity at around 85-90 Kelvin	• **Demonstrated precise control** over growth conditions • Consistently transitioned at around 85-90K
Fabrication-Ready Wafers	• **Repeatable results** on 3-inch substrate (100) LaAlO3 • Be **compatible with Silicon** and other substrates • Be ready for Josephson junctions • Be **scalable to larger wafers and yields**	• Results and analysis were consistent across multiple 3-inch wafers • Compatible with standard Silicon fabrication • A-axis HTS trilayer fabrication is easier than c-axis HTS fabrication because c-axis grown structures are not trilayer • Multiple JJ fabrication trilayer projects are underway • Larger wafers and yields can be obtained using buffer layer technology
High-Quality A-Axis Crystals	• Use X-Ray Diffraction ("XRD") • Use Scanning Transmission Electron Microscopy ("STEM") • Be more than 90% a-axis	• XRD was consistent across all samples • STEM indicated near-perfect trilayer interfaces • Images revealed more than 95% a-axis • One sample was 100% a-axis, even under STEM
Root Mean Square ("RMS") Roughness	• **Surface roughness affects yield and electrical performance** • Use Atomic Force Microscopy ("AFM") • Less than 1nm is comparable to high-quality silicon wafers	• Consistently obtained less than **1nm roughness** • Lowest obtained roughness was **0.62nm, a significant reduction from the 11.3nm roughness in previous research**
Sharp Interfaces	• ***Sharpness and thinness are required for good transport properties and quantum tunneling*** • Use STEM	• **Images revealed near-perfect, sharp interfaces** • YBCO and PBCO interfaces were smooth, thin surfaces • **An independent industry STEM expert stated that our images are as good or better than anything seen in previous literature**

Prototype Partners

ASU

NASA JPL

Polytechnic Institute — State University of New York

Cornell University — Founded A.D. 1865

Carnegie Mellon University — Pittsburgh Pennsylvania 1900

University of Waterloo — Concordia cum Veritate

Universitas Dalhousiana — Halifaxiæ N.S. MDCCCXVIII

Department of the Navy — United States of America

NIST

BROOKHAVEN NATIONAL LABORATORY

L3HARRIS™ FAST. FORWARD.

BECKERMUS The Art of Technology

LOCOMOTION

STAR CRYOELECTRONICS

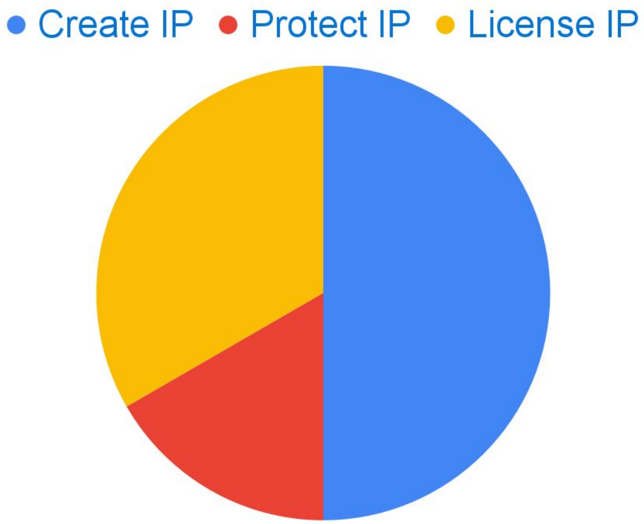
IQE

Military Ecosystem

Financial Metrics

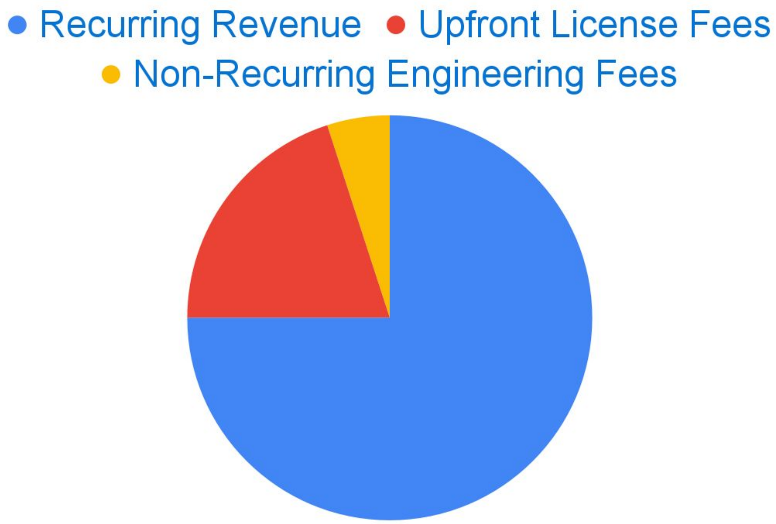
Business Model

Similar to Arm Holdings, Alphawave, and Graphcore (fabless). High-growth, high-margin, predictable.



Revenue Model

Ambature's IP model can attain ~90% Gross Margins with ~50-60% Net/EBITDA.



Growth Strategy

- **Maintain our leadership in a-axis** superconductivity technology
- Expand our IP portfolio into **new markets and use cases**
- **Integrate our technology with OEM platforms** such as TSMC, Samsung, GlobalFoundries and Intel
- **Solve key industry problems** such as the need for **high-speed interconnects**
- **Increase our superconductivity transition temperature** to unlock new products
- Develop **a customer intimacy strategy** to increase our offerings over time

Chip Design Comparables

Transaction	Valuation ($BB)	Sale Price ($BB)
Graphcore	2.8	
Tenstorrent	1	
Alphawave IP	2.9	
Cadence Design Systems	41.8	
Synopsys	44.6	
SambaNova Systems	5.1	
Groq	>1	
Lightwave Logic	0.9	
Nuvia (Qualcomm)		1.4
Arm (SoftBank)		32
Arm (NVIDIA)		38

As of August 6, 2021

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AMBATURE

www.ambature.com