

**American Semiconductor Innovation Coalition (ASIC)  
in response to Department of Commerce  
RFI 2022-01305**

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## Preamble

Semiconductors are the foundation to essential technologies – from smartphones and computers to military assets and national security systems. However, the rise of global competition and increasing complexities of geopolitics creates uncertainties in the global supply chain. Additionally, while the United States leads the world in semiconductor research, design, and tooling, there is no integrated, collaborative capability between industry, academia, and government in advanced development, prototyping, and packaging. This necessitates that the U.S. commit to restoring, driving, and scaling U.S. semiconductor and packaging leadership.

The Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Act presents a critical opportunity to define a new era of American technology infrastructure and competitive market advantage. As we undertake these historic investments to catalyze the U.S. semiconductor industry, unprecedented developments in innovation are also changing the semiconductor landscape. For example, heterogeneous integration of chips in a compact, advanced package represents a paradigm shift of extraordinary technical potential and an opportunity for U.S. technical leadership. The time is ripe to invest accordingly.

To meet this sense of urgency, a comprehensive approach should be undertaken. The American Semiconductor Innovation Coalition (ASIC)<sup>1</sup>, with broad representation of industries, small companies, universities, colleges, consortia, and nonprofits, and with technical advice from national labs, offers responses to the Department of Commerce RFI 2022-01305. The key principles below outline critical aspects to bolster a robust domestic semiconductor supply chain that is achievable, scalable, and sustainable. It should:

- Comprise a coalition of industry, academia, government (including national labs), non-profits, and start-ups to provide an innovation ecosystem with first-class resources for research, development and prototyping.

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<sup>1</sup> <https://asicoalition.org/>

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- Create and execute an ambitious, but practical, technical agenda focused on the technology transition from innovation to commercialization at scale, with a focus on technologies that can be prototyped within five (5) years.
- Tightly coordinate and align the National Semiconductor Technology Center (NSTC) and the National Advanced Packaging Manufacturing Program (NAPMP) to provide an integrated program that crosslinks expertise and leverages existing resources for maximum effectiveness.
- Be structured as closely coordinated hubs and centers of excellence (CoEs) that span the entire country and include access to resources, scientists, facilities, and partners who can work quickly and efficiently to demonstrate and transfer breakthrough technology to manufacturing.
- Leverage and upgrade prior infrastructure investments<sup>2</sup> to increase the pace of innovation by expanding existing piloting and prototype integration centers.
- Provide accessible intellectual property (IP) to accelerate technology demonstrations and prototyping.
- Set standards to enable an open chiplet<sup>3</sup> ecosystem and prioritize specific technologies for U.S. leadership, such as Advanced Heterogeneous Integration (HI), Memory, and System in Package (SIP).
- Have an inclusive governance structure based on a tiered membership model for a strong, diverse, and reconfigurable network.
- Create efficient labor markets to support nation-wide skills development and education standards, training programs guided by NSTC and NAPMP, and hands-on training facilities and design resources.

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<sup>2</sup> Accelerating Semiconductor Research, Accelerating America: Bringing the Best Development to the National Semiconductor Technology Center, February 2022 [https://www.ny.gov/sites/default/files/2022-02/Accelerating\\_Semiconductor\\_Research\\_Accelerating\\_America\\_Final%202.16.pdf](https://www.ny.gov/sites/default/files/2022-02/Accelerating_Semiconductor_Research_Accelerating_America_Final%202.16.pdf)

<sup>3</sup> Chiplet packaging allows technologies to be mixed and matched at the package or card level for enhanced functionality.

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- Facilitate start-ups and workforce development programs with access to prototyping facilities and other resources that increase and diversify the critical pool of talent.
- Modernize educational content to align with new industry needs, led by cross-agency and joint industry-academia-government partnerships to expand outreach across all background and education levels, including “new collar”.
- Ensure a sustainable long-term roadmap to achieve and sustain a domestic semiconductor supply chain.

The boundary between semiconductors and packages is blurring. The classic partition among design, wafer fab, packaging, and system integration are quickly becoming obsolete and ineffective. For maximum benefit to the country, NSTC and NAPMP ought to be closely coupled and tightly coordinated. ASIC proposes to achieve the research, development, prototyping, and manufacturing transfer goals of the NSTC and NAPMP through an integrated program that crosslinks expertise and leverages existing resources for maximum effectiveness.

NSTC needs to be the driver for full stack solutions. It should define the challenges to work on, create the technology network (academia through industry) to address challenges, and be responsible planning and execution. The Hubs are critical elements to provide project integration across the network and to fulfill the prototyping mandate of the NSTC & NAPMP. A Hub is a central facility with state-of-the-art fabrication capabilities, a link to manufacturing, and a flexible infrastructure that can support innovative technology demonstrations.

CoEs should reside at strategically selected satellite locations leveraging existing local infrastructure, skills, and ecosystems. A CoE is focused on advancing specific key technologies to a maturation point when they are transferred to the Hub for integration and demonstration. CoEs will include universities across the U.S. as a source of innovations and start-ups with a five (5) to 10-year horizon, and for education and workforce development programs that will increase and diversify the pool of talent available to industry. To this end NSTC and NAPMP should upgrade the infrastructure and programs at key universities to reduce the time and risk for tech transfer and to facilitate workforce investment.

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The CHIPS Act, as embodied in the Senate's United States Innovation and Competition Act and the House's America COMPETES Act, has the potential not only to restore U.S. semiconductor research, development, prototyping and manufacturing, but also enable the U.S. to outpace the global market competition. ASIC is proud to be part of this meaningful endeavor and looks forward to additional collaboration and partnership as we mobilize and revolutionize the semiconductor industry.

## NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER

### Question 1: Attributes and Key Factors

1. Based on the functions outlined in Section 9906 (c) of the NDAA the Department's current vision of the NSTC is as a hub (or multiple hubs) of talent, knowledge, investment, equipment, and toolsets that tackles Moore's Law transitions, post-CMOS research into new materials, architectures, processes, devices, and applications, and that bridges the gap between research and development (R&D) and commercialization.

**Question 1a:** What attributes are most important for the NSTC to possess or provide to the community (e.g., ease of access, a broad suite of leading-edge tools managed as central facility, a collaborative research environment)?

#### Response:

Today, the U.S. leads the world in semiconductor research, design, and tooling, but there is no integrated, collaborative capability between industry, academia and government in advanced development, prototyping and packaging. We have identified five key attributes for the NSTC that we believe will allow it to provide comprehensive, leading-edge support for lab-to-fab transition.

The first attribute that the NSTC needs to provide is collaboration and objective governance to serve as a link between academic research, government R&D labs and programs, company-specific R&D, and product manufacturing. The NSTC should be a collaborative entity including industry (large, medium, and small companies), government, and academia (universities and colleges). Industry, with the most thorough, up-to-date technical, process and market knowledge should have a particularly important voice in guiding and prioritizing the work in the NSTC. The NSTC should provide governance and infrastructure management through "Hubs," where stakeholders communicate and collaborate to drive a common technical agenda.

The second attribute that the NSTC needs to possess is a "full stack" integrated offering with "Hubs" connected to Centers of Excellence (CoE) around the country. The overall body should have a coordinated, integrated technology agenda. For the full potential of future technologies to be created and manufactured in the U.S., coordination across the "full-stack" must be orchestrated



at the research and development stage. “Full-stack” refers to a semiconductor chip from the materials and devices (e.g., transistors) to packaging and interfaces (which connect chips to each other and to the outside world), and the design and software tools that are used to design chips and allow them to function. Currently, most entities in the U.S. semiconductor ecosystem focus on a subset of the “stack” with no coordinating entity. This reduces the ability to commercialize and scale innovations. Moreover, the traditional boundaries between semiconductor wafers and packages are moving and evolving rapidly as blended technological concepts emerge such as heterogeneous chiplet integration. Thus, the classic partition among design, wafer fab, packaging, and system integration are quickly becoming obsolete and ineffective. As a result, we recommend tightly linking the technical agenda and the physical location and management of the NSTC and the NAPMP to bring the best research and development in both areas together.

The third important attribute that the NSTC needs to provide is an open ecosystem including a wide variety of stakeholders engaged in semiconductor research and development across the U.S. and trusted nations. This can best be achieved through one or more Hubs which serve to integrate and coordinate the activities of specialized CoEs. The ecosystem stakeholders include:

- Researchers (university, government, and industry, including start-ups) to collaborate in developing new technologies, to ensure “lab-to-fab” transfer, and educators to contribute to workforce development.
- Providers (producers, including start-ups, of semiconductor design, manufacturing, and test and measurement equipment, software, or materials) to integrate new technologies into commercial offerings.
- Users (IP developers, fabless companies, system developers, and start-ups) to collaborate in assessment of new technology tools, features, and architectures, and drive technology development toward offerings that they can adopt for their products.
- Manufacturers (companies that manufacture and package semiconductor chips and associated technology) to scale the new technology to commercial production.

The fourth attribute that the NSTC needs to provide is a full-scale, ecosystem- and partner-friendly, prototyping facility to link technology development to high-volume manufacturing. This will require a world-leading state-of-the-art prototyping facility with end-to-end advanced fabrication capabilities as well as flexible infrastructure which can support innovative prototypes. It should be built primarily on an existing advanced 300 mm microelectronics research fab with full flow capability, including state of the art metrology, inspection, characterization, electrical testing, reliability testing, physical failure analysis, assembly, and packaging.

To be operational from day one, the NSTC must leverage a range of existing assets, including baseline fabrication flows and existing R&D centers. The necessary attributes of the prototyping facilities include:

- 24-7 staffing and the operational discipline and procedures to support rapid cycle time.
- A successful history of technological innovations, collaborations, prototypes, and customer programs.
- Assignees from member companies working on-site to contribute to the common ecosystem, not in separate sandboxes.
- Leading edge equipment capabilities and tooling (design, manufacturing, measurement and test equipment, software, and materials).
- Sufficient background IP (flows, mask sets, etc.) to leverage existing know-how for the common good and to hit the ground running.
- Contamination protocols to ensure quality, but with sufficient flexibility to allow wafer exchange with other locations (fabs, labs, universities).
- “Flex space” or “flex tools” with ability to swap out materials and processes to support a wide range of experimental needs and to bridge lab-to-fab. These may be in a segregated part of the fab for contamination protocols, or chambers on existing tools, among other possibilities.

The fifth attribute that NSTC needs to provide to the community is an environment that fosters workforce development across the nation. Semiconductor ecosystems are enabled by the diverse and constantly evolving talents of American workers. The NSTC and NAPMP should open doors to inclusive, well-paid jobs across the U.S by collaborating with universities, community colleges and industry to build skills pathways to jobs in the semiconductor industry. The following components would support workforce development in the semiconductor industry:

- Apprenticeship programs with paid, hands-on learning for advanced careers in the semiconductor industry.
- An academic network partnered with industry across the U.S. to create more semiconductor technology education opportunities at all educational levels.
- A focus on underrepresented communities.

**Question 1b:** What key factors are critical for the NSTC to address the current gaps in the semiconductor R&D ecosystem?

**Response:**

The key factors critical for the NSTC to address the current gaps in semiconductor R&D ecosystem can be articulated around the following 4 pillars of activity as defined in the CHIPS legislation: Manufacturing R&D, Packaging R&D, Design R&D, and Demonstration and Prototyping.

**Manufacturing R&D is needed for** focusing on next generation beyond-FinFET logic technology and interconnect scaling for the 3nm node and below, including advanced memory scaling, analog/mixed-signal technology and custom enhancements of existing technologies, as well as RF and high-power materials and devices. This pillar should be based on a domestic, open, and precompetitive infrastructure. It includes advanced process development including environment-friendly technology development, with characterization, instrumentation, and testing for semiconductor devices and for the materials used in fabricating the masks, interconnect, and packages for chipllets at advanced nodes. An essential element will be to provide design

enablement, i.e., modeling and process design kits (PDKs). The successful results of this research can be transferred to domestic foundries and packaging facilities for use in volume manufacturing. This pillar should also include research on the virtualization and automation of tool maintenance, including AI/ML and digital twins, for advanced fabrication and packaging, and development of methods for measuring and analyzing manufacturing data for security and supply chain verification, with specialization at appropriate regional Centers of Excellence.

**Packaging R&D is needed** for a next-generation heterogeneous open chiplet ecosystem and 3D integration, bond, and assembly including optical interconnect. Chiplet packaging allows technologies to be mixed and matched at the package or card level for enhanced functionality. This pillar should also include development of advanced packaging substrates, bond and assembly materials and techniques to achieve high-density interconnectivity between chiplets, high off-module connectivity such as through optical interconnects, and the establishment of open standards for chiplets.

**Design R&D is needed** including beyond-CMOS computing, chip/package co-optimization, and design/system-technology co-optimization (DTCO & STCO). Development of electronic design automation (EDA) tools is necessary for next generation logic, interconnect, and packaging, including artificial intelligence and machine learning (AI/ML) methods for enhancing design productivity and quality. There is significant design work that touches upon many aspects of the semiconductor supply chain and activity should cover architecture and SOC methodology for design portability across fabs, design support for power delivery and management in advanced nodes and packages, co-design with stacking and advanced packaging, application-driven co-design of accelerators and SOCs, design and architecture for hybrid technologies (e.g., processing in memory), architecture and protocols for multi-chiplet heterogeneous systems, design for supply chain security and integrity, advanced node circuit design and optimization, SOC architecture for photonics. Work in these areas can allow the development of novel, reusable IP to accelerate the adoption of new semiconductor technologies. For collaboration, especially with start-ups, a secure hybrid multi-cloud design platform is needed to encourage cooperative projects, including the porting and reuse of design IP, with design, simulation, and verification tools. The design platform can also serve as a testbed for cloud modernization of EDA tools and flows to enable more resource-efficient and flexible design activity for new computing workloads. This pillar should

also include development of open-source EDA tools to reduce barriers to access and as a feeder for commercial EDA.

**Demonstration and Prototyping** facilities and services are necessary to validate novel approaches and for industry consumption of all the above technologies in advanced research fabs and manufacturing sites. Providing PDKs, multi-project wafer (MPW) runs, and early user hardware through the NSTC and NAPMP network, including partnerships with commercial manufacturers, can create a fast track to production. For example, Hubs should have a full suite of fully enabled, leading-edge, industry-relevant 300mm processing, metrology, testing, and failure analysis tools capable of advanced node CMOS development with 24/7 pilot line operation, building on the current infrastructure. The demonstration and prototyping capability should include engineering short loops for specialty technology and IP as an essential step toward proving and maturing new technology elements. Differentiated back-end technologies, such as advanced embedded memory for AI and other new data workloads on top of commercial transistor technology from U.S.-based foundries, can also be enabled. In addition, any given distributed CoE may utilize specialized technologies for analog and mixed signal enabling rapid experimentation on 200mm tools (as these are still widely used in AMS applications) covering a wide spectrum of materials and processes. Once matured, these elements will be transferred for integration at the Hub.

## Question 2: IP Approaches and Issues

2. As authorized, the NSTC would have to be able to work with a wide range of research groups from industry, academia, and government, some of whom will be contributing valuable intellectual property. What approaches to intellectual property should be in place to protect the foundational contributions of members while enabling maximum collaboration and innovation amongst the research community supported by NSTC? What IP issues create unique challenges for middle- and late-stage prototyping collaborations versus early-stage research, design and proof-of-concept collaborations?

**Response:**

Clearly there are multiple NSTC objectives: generating and protecting IP, maximizing collaboration, accelerating commercialization, and leveraging industry capabilities. These objectives should be considered overall, while recognizing that there are important aspects for different constituencies. The NSTC setting should support a flexible public-private partnership to enable start-ups, university, commercial and non-traditional participants to engage. In doing so, the NSTC will face with the unique challenges in managing the IP goals of all member sectors needs for all stakeholders including government, industry, and academia. To achieve the goal of NSTC of maximizing collaboration and driving innovation to commercialization, a stakeholder-tuned IP approach will be needed. The goals of these organizations may not necessarily align, but all parties will need to work together to achieve the goal of NSTC's goal of maximizing collaboration and driving innovation to commercialization.

The IP general principles should allow partners to collaborate on R&D challenges and drive towards prototypes. Another high priority is to promote the growth and nurture of start-ups. The IP principles should also recognize that in the breakthrough research phase more generically applicable results will be achieved. This phase calls for more flexible and broad sharing arrangements than when approaching the prototype phase. During prototyping, application and partner confidential information will enter the innovation process.

When building the partnership, contracting parties should strive to adopt general IP principles and aspire to optimum sharing and the widest possible use of results. However, where appropriate, the NSTC rules should allow maximizing the value for the individual stakeholders by agreeing on program/project specific IP rules in their contracts.

Start-ups: By their very nature, start-ups have unique IP needs. Start-ups participating in the NSTC should not be required to share their IP with established industry in the coalition as this could jeopardize the start-ups' ability to obtain the next round of funding (investors could see the established industry as being able to outpace the start-up in reaching the final product goal). Start-ups should be incentivized to join the NSTC and have access to licensing coalition IP that they need to practice their own IP. The NSTC should further support start-ups by providing access to standard tool sets (physical and digital, electrical, and mechanical) and prototyping runs so they

can demonstrate the value of their IP more rapidly. An NSTC affiliation and the support that it demonstrates will help start-ups secure financial support by the venture community.

**University:** Universities will bring considerable relevant background IP with their participation in the NSTC. This IP may have been generated through research funded by non-NSTC resources and may have co-inventors which may or may not actually participate in the NSTC. As appropriate, universities must disclose the applicable background IP of participating Principal Investigators and whether that IP is available for commercial licensing to the NSTC. The existence of university background IP can clearly signal a valuable reservoir of expertise and the universities' ability to contribute towards the technical agenda of the NSTC. Therefore, the existence and availability of university background IP should not be used to block the participation of a university in a given technical area.

Foreground IP that is solely produced by university personnel using university facilities and university administered funding is solely owned by the university. Assuming that the NSTC will commingle government and industry financial resources, within a limited period of time, the NSTC or any member of the coalition has an option to non-exclusively commercially license this university foreground IP under various licensing modes using reasonable and non-discriminatory terms. Once that option lapses, the university should be free to license the IP exclusively or non-exclusively to a third party including a start-up. If university project funding comes from the U.S. Government only, university foreground IP may be managed under standard Bayh Dole regulations.

Foreground IP that is jointly created by university inventors and company coalition inventors should be jointly owned by the university and the co-inventors from the NSTC. Any coalition member or the NSTC as a whole will have a period of time to license the technology commercially and non-exclusively under RAND terms. Once this period lapses, the parties may license the IP to a third party such as a university start-up, exclusively or non-exclusively.

**Industry:** Industry will likely contribute foundational IP in design, process, integration/architecture, equipment, materials, test, cybersecurity of manufacturing and devices, and many other categories. A flexible licensing framework to protect and allow foundational, background IP to be licensed (when free to do so) broadly to members for early-stage research and

prototyping collaborations with reduced barriers of entry and on a RAND basis for late-stage prototyping and path to commercialization should be established.

The parties could consider having some part of NSTC funding go towards providing a baseline process design kit which could be freely licensed to NSTC member entities for a given set of fab infrastructure. This should not be limited to cutting edge PDK and should focus on including process modules developed using NSTC funding.

Considerations for basic consortium IP policy could include a number of innovation approaches as described here:

- If IP is developed by a single participating company, that company owns and keeps their IP,
- If IP is generated jointly among two or more NSTC, i.e. “consortium” members, that IP is jointly owned IP,
- IP licensing to consortium members is encouraged,
- Provisions are made for “evaluation licenses” where consortium members can, for a pre-determined period of time and for no license fee, try out consortium developed IP for themselves in pre-production assessment (not for commercial use),
- Participants must disclose when they make an invention disclosure or file for a patent when making use of joint research results under NSTC funding,
- If a participant inventor decides to abandon or not pursue filing a patent on consortium developed IP, the U.S. government has the right to pursue a patent,
- It would be useful to include the concept of the right of first refusal in the basic principles.

In all cases, commercial licensees (whether NSTC participants or start-ups) must demonstrate the technical and financial capabilities to develop the early-stage technology into commercially successful products and should diligently pursue commercialization.



### Question 3: Interface and/or Incorporate Existing R&D Initiatives

3. The federal government has several programs that support microelectronics and associated R&D across many agencies, federal labs, university labs, corporate labs, and other for-profit and nonprofit entities.

**Question 3a:** What existing domestic R&D activities, assets, intellectual property, knowledge and expertise should be incorporated or otherwise connected to the NSTC, and are any international in nature?

**Response:**

We recommend that a university network be envisioned for the NSTC and NAPMP that conducts advanced R&D and feeds a pipeline of innovative technologies focused on prototyping through the Hubs and CoEs. In addition to the universities, national labs and start-ups will play a vital role in the R&D pipeline within the NSTC and NAPMP network. National labs have many unique capabilities for materials characterization (e.g., beamlines for state-of-the-art x-ray techniques) as well as wafer scale fabrication capabilities including non-CMOS materials such as III-Vs, etc. Furthermore, national labs have the ability to integrate new technologies developed in the NSTC into system architectures for defense applications thereby fulfilling a critical Department of Defense (DoD) need. As envisioned in the response to Q1, the Hubs provide the central facility with key capability, e.g. 300mm state of the art equipment that will execute all of the advanced prototyping activities, such as NY CREATES' world-class 300mm pilot facilities in Albany, New York. This site is part of the New York's semiconductor ecosystem and is a product of billions of dollars in public and private investment<sup>4</sup>. The CoEs may be focused on specific development activities with limited equipment and capabilities that will develop and mature new technologies to the point where they can be transferred to a Hub for advanced prototyping thereby ensuring a "lab-to-fab" transfer. There could be several Hubs and CoEs depending on technology area with

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<sup>4</sup> Accelerating Semiconductor Research, Accelerating America: Bringing the Best Development to the National Semiconductor Technology Center, February 2022 [https://www.ny.gov/sites/default/files/2022-02/Accelerating\\_Semiconductor\\_Research\\_Accelerating\\_America\\_Final%202.16.pdf](https://www.ny.gov/sites/default/files/2022-02/Accelerating_Semiconductor_Research_Accelerating_America_Final%202.16.pdf)

multiple workstreams defined.

Each CoE workstream would consist of technical thrusts with participation from the broader national/international academic community and academic participants chosen via a competitive project proposal process. From this process, each thrust would determine its academic participants and appoint an academic director (who has significant autonomy and discretion similar to the DARPA/SRC JUMP Center directors). Universities with incumbent facilities and capabilities that are aligned with the NSTC and NAPMP activities should be candidates for infrastructure funding. This will enable these universities to engage in technology path finding and transfer into the NSTC and NAPMP hubs in addition to hands-on student training and other NSTC participants including start-ups. University infrastructure investment decisions through the NSTC and NAPMP should be made jointly with academic and industry partners to ensure alignment with the technology agenda as well as the workforce development workstream. University infrastructure investment decisions will require a survey of existing capabilities. The focus of the activity around the Hubs and CoE will be within the U.S., however, collaborations with similar institutions within allied nations, e.g. the EU (Fraunhofer, IMEC) can be pursued as well.

**Question 3b:** How should the NSTC interface with federal labs, university labs, corporate labs and other existing institutions of R&D and prototyping to ensure that R&D projects are supported throughout the technology maturation process so that public research funds are able to improve R&D productivity and attract additional private and venture investment?

**Response:**

It is important that a management structure for the NSTC and NAPMP include several key elements:

- (a) As discussed in response to Question 1, the NSTC should be a collaborative entity including industry, government, and academia. Industry, with the most thorough, up-to-date technical, process and market knowledge critical for scale up and prototyping should have a particularly important voice in shaping and prioritizing the work in the NSTC.

(b) The university network should be managed by a dedicated entity within the NSTC and NAPMP that responds to a board of representatives from government, industry (including start-ups), non-profits and academia.

(c) The board should have great discretion and autonomy and give voting rights for project selection with appropriate weighting to industry (large, medium and small companies including start-ups), government (including defense industrial base), and academia.

The focus of the R&D activities should be to enable advanced prototyping to differentiate and enhance the NSTC and NAPMP project portfolio. Therefore, all R&D projects need to have a five to ten-year horizon to strengthen U.S. semiconductor manufacturing. The funding from the NSTC and NAPMP for the university network, especially for the academic partners, should be aimed at R&D projects and infrastructure investments within selected academic institutions to enhance R&D interactions between academia and NSTC and NAPMP. The university network would have autonomy with respect to activities within their facilities that are related to the federally funded program (NSTC and NAPMP). The university participants along with the national labs should also be able to engage in collaborative work in advanced technologies within the Hubs and CoEs.

The NSTC and NAPMP also needs to be tightly linked to the US semiconductor manufacturing ecosystem, especially the new and upgraded facilities to be supported by Sec. 9902 of the FY2021 NDAA. The impact of technologies on U.S. manufacturing that will be developed and prototyped by the NSTC and NAPMP will be an important contributor to the long-term viability and sustainability of this model. If manufacturers see value in the technologies being developed in the NSTC, they will continue to be active supporters, funders, and sources of skilled assignees for the long term.

#### **Question 4: Connection with National Network Semiconductor R&D**

4. How should the NSTC connect to the National Network for Semiconductor R&D, authorized in Sec 9903 of the FY2021 NDAA?

**Response:**

It is critical that the research agendas and technical capabilities of the commercially focused NSTC and NAPMP and the DoD funded National Network for Microelectronics Research and Development (NNMRD) be coordinated. Both DoD and commercial companies are united in their need to identify viable emerging technologies, including those containing novel materials and devices, circuits and architecture, of high impact to the semiconductor supply chain, start-ups, and the manufacturing eco-system. Therefore, the university network of the NSTC and NAPMP which conducts advanced R&D and feeds a pipeline of innovative technologies for commercial prototyping should have strong synergy with the research agenda and workforce development focus of the NNMRD. Thus, close coordination of infrastructure investments within the university community will be needed to avoid duplication and maximize broad leverage across programs. Additionally, security and protection of domestic IP are concerns shared by both commercial and defense programs. However, the NSTC and NAPMP should be focused on commercial industrial leadership and should not be affected by defense-specific security, International Traffic in Arms Regulations (ITAR) restrictions, or niche defense needs. Mission areas that DoD values highly but are not as applicable to industry may also be identified for NNMRD focus. Dual use and viable technologies and designs matured through the NNMRD can be developed further and tested out through prototyping within the NSTC and NAPMP and readied for transfer to manufacturing facilities. It is essential that any trusted/assured requirements for DoD technologies be comprehended early on in the planning phase for the NSTC and NAPMP to minimize impact on physical layouts, IT security, and personnel issues.

**Question 4a:** What considerations should be given to ensure strong interaction between the two efforts?

**Response:**

There must be tight cross-agency coordination focused on the strategic implications of the future of semiconductors. An important distinction between the DoD work and that of the NSTC and NAPMP is that DoD will also likely include work at the classified level, while the NSTC and

NAPMP will have a commercial focus. National labs can also play a critical role since they have the ability to integrate new technologies prototyped in the NSTC into system architectures for defense applications, thereby fulfilling a critical DoD need. To the extent possible, it would be useful if both DoD efforts and the NSTC and NAPMP could use similar tools, techniques, flows, etc. to avoid fundamental obstacles from crossing over from one to the other.

Intra-agency coordination is also needed. For example, DARPA alone has multiple semiconductor related research projects in addition to its ongoing portfolio of MTO projects. These include programs such as:

- DARPA Electronics Resurgence Initiative (ERI): Government-industry partnership investing to support a domestic semiconductor manufacturing sector that implements specialized, secure circuits that can be trusted through the supply chain. This comprises 3D heterogeneous integration, new materials and devices, specialized functions, and design and security. It includes participation from industry, defense, and academia; and
- DARPA Joint University Microelectronics Program (JUMP): Partnership between DARPA and the Semiconductor Research Corporation working to increase the performance, efficiency, and capabilities of electronic applications.

Additionally, beyond the NSTC/NAPMP/NNMRD coordination, there are multiple US government initiatives in NSF, DoE, DoD and DoC to promote semiconductor innovation and production. It is very important that these programs be coordinated and integrated into a cohesive national strategy. In particular, it is imperative that through the aggregate of these programs, suitable investments in the university microelectronics infrastructure are made that enable universities to carry out their critical functions. The different priorities, strategies, incentives, and culture of the multiple agencies involved makes this type of coordination complex but critical for the U.S. to optimize its investment strategy.

**Question 4b:** Should there be overlap in the technology readiness levels served by each program?

**Response:**

Yes. To bridge the so-called “valley of death”, a funding and resources gap between “lab to fab”<sup>5</sup>, a tight connection between the DoD NNMRD and the university network of the NSTC and NAPMP is needed. This synergy would allow the identification of dual use technologies across the commercial and defense spaces that could leverage the advanced prototyping capabilities of the NSTC and NAPMP. Thus, an overlap of TRL levels may be required, especially between levels 3-4 where a technology has been validated in a lab. Technologies matured through the NNMRD can be transitioned into the NSTC and NAPMP for prototyping, and eventually an overlap in TRL levels 6-7 is also expected for transfer to manufacturing. Therefore, the unique capabilities of NSTC and NAPMP enable advanced prototyping and fills the gap, or missing capability, in today’s American semiconductor ecosystem, and would serve both commercial and government needs. For a seamless transition between the DoC and DoD networks, an agreed-to set of TRL definitions would also be required, as in practice, agencies define TRL’s slightly differently. In addition, the trusted/assured requirements for DoD technologies will need to be comprehended to enable secure prototyping in the NSTC and NAPMP. Finally, it should also be pointed out that while overlap of TRL may be needed, this does not necessarily imply technical overlap, as the NSTC and NNMRD may have different technology focuses.

**Question 5: Long-term Roadmap**

5. How should the NSTC ensure that it can identify and invest in what comes next after the first wave of needs are identified in the initial years?

**Response:**

The NSTC and NAPMP mandate should be to mature technologies to the point where they can be transferred to manufacturing. The Hubs and CoEs within the NSTC and NAPMP should focus on

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<sup>5</sup> American Innovation, American Growth: A Vision for the National Semiconductor Technology Center,” MITRE ENGENUITY, 2021.

technologies that can be demonstrated within a five-year horizon. However, for the long-term sustainability of the NSTC and NAPMP, a strong link between the Hubs and CoEs and the university network is needed to conduct advanced R&D to develop and identify new technologies that can be candidates for advanced prototyping within the NSTC and NAPMP. The long-term R&D network should focus in a five to ten-year timeframe.

In addition, a flexible and agile framework is required to enable timely capture of changes and new additions to the technology roadmap and for these to be communicated to the NSTC and NAPMP participants on a regular basis. NSTC and NAPMP will possess a breadth and depth of knowledge from its participants that can be leveraged to develop a roadmap of key technologies and inflections associated with such technologies. NSTC and NAPMP will decide on the overall location, ownership, mission and number of affiliated CoE and Hubs.

Roadmaps should initially cover advanced logic, analog/mixed signal, DRAM, 3DNAND, emerging memories, key process technologies (especially lithography) and heterogeneous integration including open chiplet ecosystem across key application spaces such as HPC, 5G and AI. Beyond the first 5 years, new solutions for the U.S. will need to be created. NSTC and NAPMP will have to engage and align with the various U.S. technology feeders. These feeders include the NSTC/NAPMP university network (as described in the response to Question 3), workshops, the DoD National Network for Microelectronics Research and Development (NNMRD), the SRC through its 2030 Decadal Plan for Semiconductors<sup>6</sup> and other government R&D inputs such as from DARPA and national labs.

**Question 5a:** To what extent does the semiconductor ecosystem need a long-term roadmap of application requirements, technical needs, and gaps in materials, tooling and equipment, and process capabilities in order to guide future R&D investments?

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<sup>6</sup> <https://www.src.org/about/decadal-plan/>

**Response:**

History has shown that the semiconductor industry uses roadmaps to maintain reference points and calibrate technology discussions across the industry. Roadmaps give a common baseline and reference points for dialogue between companies and are used to define and propose standard approaches that enhance the speed of innovation. They can be used by companies while they define their own product roadmaps and by universities for grant applications. An integrated view of the roadmap across core technologies such as logic, memory, analog mixed signal will accelerate material, equipment, and design tool availability to the entire ecosystem, driving value creation across the entire supply chain. The NSTC and NAPMP should align their activities with evolving technology trends and aim to stay ahead of them. A priority activity could be around a heterogeneous integration (HI) roadmap where the lack of common goals and standardization is currently a limiting factor for product innovation. In particular, recent roadmapping initiatives, including the International Roadmap for Devices and Systems (IRDS) and IEEE HI roadmaps (which have strong international participation) should be leveraged. Additional input from the NNMRD and university network would be valuable.

The timely identification of long-term technology inflections will enable a focus for the NSTC and NAPMP prototyping activities that align with and support industry needs and enable down selection of potential technology options in a timely and cost-effective manner. Future NSTC and NAPMP investments need to be focused on significant challenges identified in the new roadmap. The NSTC and NAPMP roadmap update should be part of the standard business process and annually report to the executive body accountable for NSTC operation.

A NSTC and NAPMP roadmap and strategy should be in place as the result of the aforementioned stakeholders' interactions and assessments, with frequent public releases of the aggregated elements in large symposia and through NSTC and NAPMP Technology Reviews. These roadmaps indicate opportunities and challenges without being explicit regarding the solutions and IP behind these.

Finally, it should be noted that the university network within our vision of the NSTC is playing a critical role in pathfinding and identifying key technology trends. The university network activities will be closely aligned with direction from the industry members of the NSTC to identify key



technologies for advanced prototyping within the NSTC facilities that can impact and differentiate U.S. chip manufacturing.

**Question 5b:** How can the NSTC’s investments best support an open roadmap of this type, and how should the NSTC interface with other governments or allied international R&D programs, such as those established under Section 9905 of the FY2021 NDAA, to enable such a roadmap?

**Response:**

NSTC & NAPMP should align closely with similar activities overseas e.g. the emerging activity for funding the European CHIPS act, and similar measures with Asia-Pacific allies, such as Japan and South Korea. The NSTC and NAPMP should consider partnerships with IMEC and other institutions like Fraunhofer Institute and CEA-LETI to broaden and align U.S. domestic entities with our allied countries. Ultimately, NSTC and NAPMP should develop a mechanism to establish joint research collaborations with companies in allied countries and allied governments to ensure a common technology roadmap and open-source and cost-effective platforms.

Furthermore, the vision of the NSTC should comprehend and be informed by the Multilateral Semiconductor Security Fund envisioned in Section 9905 of the 2021 NDAA. This could be in several forms, including research and development in novel security techniques that could contribute to the Fund’s mission, and in setting guidelines for supply chain security and international interaction with allied countries that might be needed when NSTC is collaborating with other entities on research and prototyping programs.

**Question 5c:** What existing technology forums, roadmaps, or other initiatives should be incorporated into such efforts?

**Response:**

The SRC Decadal plan describes the key five seismic shifts over the next 10 years around novel analog electronics, memory and storage, energy efficient communication, energy efficient

computing, hardware enabled security and will be a critical initiative to be incorporated into the roadmap activity. In addition, the IEEE HI Roadmap<sup>7</sup> will be complementary and bring in the advanced packaging perspective. Specific industry input that incorporates emerging workloads that need demonstrators to evaluate the viability of the advanced technology will also need to be comprehended.

### Question 6: Public-Private Partnership

6. The NSTC is envisioned as a public-private partnership. What are the most suitable models of public-private partnership for the R&D and prototyping gaps that the NSTC is envisioned to address?

#### Response:

A public-private partnership for R&D and prototyping is essential to meet the government's goals of ensuring the U.S. semiconductor leadership and to accelerate innovation. Only by bringing together all stakeholders from the ecosystem will the NSTC and NAPMP be able to effectively drive growth and safeguard our country's competitiveness.

Several public-private models have emerged in the last few decades that can serve as inspiration for the NSTC. We offer the following recommendation based on analysis of best practices of a few successful models – the National Network for Manufacturing Innovation (or Manufacturing USA), NY CREATES and imec.

The NSTC should implement a networked model of a hubs with multiple Centers of Excellence (CoEs), including universities. The NSTC hub provides central oversight and overall coordination across all CoEs to drive focused acceleration of the NSTC mission, as well as to manage cross-CoE programs such as workforce development and start-up support. The NSTC hub is also responsible to manage the links and connections of NSTC to other research efforts in the

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<sup>7</sup> <https://eps.ieee.org/technology/heterogeneous-integration-roadmap.html>

government including the proposed expanded NIST metrology program and Manufacturing USA Institutes, and the DoD Microelectronics Commons.

Each CoE should focus on specific semiconductor technology areas as defined by the overall technical agenda, such as advanced logic, memory, heterogenous integration, analog/mixed signal (AMS), etc. These CoEs should be strategically located around existing U.S. semiconductor locations to leverage existing specialized technical equipment and talent, as well as partner ecosystems such as material suppliers, equipment vendors, design houses, universities and at-scale manufacturers.

**Question 6a:** What are the roles of the public participants and the private-sector participants in this partnership, including any international participants?

**Response:**

All participants should be active in the engagement through staffing, funding, IP, and research. By committing to the mission, there would be fundamental gains to the members leading to the success of the NSTC. Public sector participants can serve as a neutral 3rd party, operate the shared facilities, and support engineering work for other NSTC participants. Regarding international participants, foreign members could participate in programs, executive committee or board of directors with the approval of DoC and NSTC board.

**Question 6b:** How should governance structures, program objectives, investment criteria, and oversight and accountability requirements be structured to maximize the transformative potential of the NSTC in the US R&D ecosystem?

**Response:**

The NSTC should be a nationwide endeavor built on technology Hubs and supporting Centers of Excellence focused on specific technology elements. Participants of the NSTC could contribute to one or more hub activities. The Hubs should pursue a technology agenda in coordination with

other hubs and the overall NSTC technical advisory committee, so that the overall NSTC technology agenda is focused and coordinated.

Any member organization which participates in an NSTC Hub roadmap must support that technology with a combination of capital, assignees, cash, IP, tools, software, or other in-kind contributions. In return, the member will get access to NSTC output and rights to use and enhance the IP generated. There may be differing levels of membership, with differing rights and obligations, depending on contribution level.

### **Question 7: Support of Both Small Co and Established Entities**

7. What operational and organizational characteristics, business processes, and practices will be important in ensuring that the resources of the NSTC are broadly accessible and available to the broader U.S. semiconductor R&D community including both small and larger, more established entities? How can the NSTC ensure that smaller and medium- sized companies and start-ups have access to facilities, expertise, and intellectual property that public funds support? What operational and organizational characteristics, business processes, and practices will be important in ensuring that the resources of the NSTC are broadly accessible and available to the broader U.S. semiconductor R&D community including both small and larger, more established entities?

#### **Response:**

The NSTC should be structured so it operates as an inclusive and seamless ecosystem for all partners from industry, academia, and government. Similar models have been demonstrated with success specifically for the semiconductor industry, such as NYCreates' world-class \$15 billion 300mm pilot facilities in Albany, New York. Building from an existing entity would enable the NSTC to leverage previous investments, know-how, and track record of developing and managing these complex and expensive facilities from day one. Avoiding the need to “reinvent the wheel” by creating new facilities or related capabilities from scratch.

A consortium model where membership is open to companies and institutions of all sizes will

allow representation from the broader U.S. semiconductor R&D community including both small and larger, more established entities. As such, to ensure NSTC's resources are accessible and available the NSTC should have 1) a strong, diverse, scalable, and reconfigurable network, 2) access to resource and capabilities, and 3) an inclusive governance structure, as described below.

### **1) Strong, diverse, scalable, and reconfigurable network**

As described in the response to Q6, the NSTC should foster an innovation ecosystem for advanced development and prototyping with leading organizations that represent all sectors (academia, start-ups, government, investment, industry) bringing together and aligning the best qualified contributors from across the country. This network should serve as a connector and access point to the broader U.S. semiconductor R&D ecosystem through an R&D Hub with multiple Centers of Excellence (CoE), i.e., akin to a hub-and-spoke model, which have been demonstrated successfully in the past from models such as Manufacturing USA.

A strongly established network will provide continuity and collaboration across the entire U.S. semiconductor R&D ecosystem, particularly on technological advancements which require integration across multiple specialty areas. This model is designed to allow key partners and contributors to have formal control and oversight of the NSTC to ensure that the perspectives and needs of all stakeholders are aligned and well represented in its key initiatives and related programming.

### **2) Access to resources and capabilities**

In support of the NSTC's mission to protect and advance U.S. leadership in semiconductors, access to existing SOTA resources and capabilities from the U.S. semiconductor community is key to a fast start. Particularly with respect to accelerating the pace of lab-to-fab and supporting breakthrough innovation, the NSTC should provide significant financial and in-kind support for discounted and streamlined access to shared-use facilities and tools for start-ups, small businesses, and medium-sized companies. It is critical that these shared facilities and bridge tools (full-scale tools required to get from research and across the "valley of death" to commercial capability without disruption to manufacturing) are accessible to the NSTC community. These capabilities should be able to pilot up to 300mm wafers to stay aligned with

the current needs of industry. These facilities and tools are typically too expensive for universities or early-stage ventures to access with conventional funding, but they are critical to the development and commercialization of most semiconductor technologies. The NSTC should organize and aggregate these various academic, government, and industry resources for qualified entities and offer them in a discounted and scalable way, akin to federal laboratory “vouchers” programs that have been successfully deployed for researchers and start-ups in the past. The government can leverage existing capabilities and reinvest in existing capabilities, such as NY CREATES’ 300mm pilot facilities in Albany, to ensure SOTA resources and capabilities can be accessed by NSTC members.

Fabrication facilities, cleanrooms, advanced equipment, subject matter expertise, and office space, should be made available to all NSTC members. The provision of an innovation ecosystem for advanced development and prototyping with first-class resources, experts, facilities and partners who can quickly and efficiently demonstrate and transfer breakthrough technology to manufacturing will be a key benefit of the NSTC. To maximize these resources’ potential, they should be deployed where NSTC members can be co-located together and thus able constantly to engage and collaborate with one another. Deploying this co-location strategy will ensure the resources of NSTC are accessible and available to the broader U.S. semiconductor R&D community including both small businesses and larger, more established entities.

In addition, one of the many barriers to entry for smaller and medium-sized companies, as well as start-ups, is the prohibitive cost of developing and securing intellectual property (IP), the building blocks of semiconductors. It is imperative that the NSTC be structured so that universities, start-ups, and small businesses are able to easily leverage IP to develop new technology and related intellectual property in a way that allows them to license that technology easily and to raise follow-on capital from investors and strategic partners. Therefore, it is critical that the NSTC and NAPMP catalyze and transfer the creation of foundational IP supported by government, commercial, and academic sources from day one. A quick and efficient way to accomplish this is for the NSTC to acquire an initial pool of IP from companies, academic institutions, and research centers and make it available to participants.

### 3) Inclusive governance structure

A major component of ensuring the NSTC incorporates industry best practices and closely tracks any changes in the global semiconductor markets, will be forming and leveraging an active and engaged advisory body for the organization. It is essential that this advisory body features a diverse and inclusive mix of globally recognized subject matter experts and thought leaders from established and emerging organizations of all sizes across the U.S. semiconductor space. The organizational and governance structure of NSTC should be designed so that the organization is closely aligned with and directly accountable to its key stakeholder groups, including industry, academia, and government. The NSTC must embrace an inclusive culture and actively seek diversity of all kinds at all levels to fuel the type of breakthrough innovation and creativity needed to develop and scale semiconductor and other microelectronics technologies. It is also critical that top talent from the key segments of industry, academia, and government with relevant experience operating and managing semiconductor fabs are tapped to lead the NSTC. The knowledge, networks, and credibility these individuals would provide to the overall effort from inception will position the NSTC more effectively for long-term success.

The NSTC’s advisory body should serve as a sounding board and seek technical advice from its members to ensure that industry perspectives and needs are aligned and well represented in the NSTC’s key initiatives and the related programming it offers for technology commercialization, workforce development, and start-ups. Members of the advisory body can also provide the added benefit of serving as informal “brand ambassadors” for the NSTC to help raise its awareness and profile within their respective networks.

**Question 7a:** How can the NSTC ensure that smaller and medium- sized companies and start-ups have access to facilities, expertise, and intellectual property that public funds support?

**Response:**

The NSTC should serve as a national engine for identifying and accelerating the best semiconductor and microelectronics-related innovations from the lab and into the market. Based

on recent trends of large, established companies backing away from licensing university-born technologies and relying upon start-ups and small businesses for initial commercialization, it is critical that the NSTC be designed to enable smaller and medium-sized companies and start-ups as they work to de-risk technologies, validate market opportunities, and build their teams. In addition, the huge amounts of capital and long lead times to market for semiconductor start-ups and smaller companies require more support from the government to position them to successfully raise follow-on capital from investors, enter into development agreements with partners, and gain traction with customers. The current levels of early-stage funding from both the government and industry to these entities are simply not sufficient (Fig. 2) and require exponential increases in order to put the U.S. and our domestic semiconductor ecosystem on a path to long-term global competitiveness and national security. Over the period of 2017-2021, Chinese venture capital funds have invested about twice the amount of their American counterparts in semiconductor companies (\$12.6B vs. \$6.6B respectively).

The NSTC should provide significant financial and in-kind support for discounted and streamlined access to shared-use facilities and bridge tools (full-scale tools required to get across the “valley of death” from research to commercial capability without disruption to manufacturing) for start-ups, small businesses, and medium-sized companies. These facilities and tools are typically too expensive for these entities to support with conventional funding, but they are critical to the development and commercialization of most semiconductor technologies. To do so, the government can leverage existing capabilities and reinvest in existing capabilities, such as NY CREATES’ 300mm pilot facilities in Albany, to ensure that these SOTA facilities and tools are made available to NSTC members with an emphasis on access to small and medium sized start-ups and companies.

Additionally, removing barriers of entry for smaller and medium-sized companies and start-ups such as the prohibitive cost of intellectual property is critical to the contribution of these organizations to the semiconductor community. The NSTC should be structured so these entities are able to easily leverage IP to develop new technology and related IP in a way that allows them to license that technology easily and to raise follow-on capital from investors and strategic partners.



**Question 8: Lessons Learned from “Research Consortium”**

8. For those who currently participate or have participated in a “research consortium” (either domestic or international) made up of public and private partners, what are the important lessons learned or best practices that the NSTC should follow?

**Response:**

We would like to articulate the answer for “research consortium” lessons learned and best practices around two topics: IP management and governance model.

Starting with IP, it is important to define with some precision the essence of “public and private” partners. Public partners will include all universities, both publicly and privately funded, as well as federal agencies and national labs. Private partners will refer to the companies (industry), both publicly traded and privately held. The private partners require IP rights, whereas the public partners want to see their work reach the marketplace. A key criteria for success is a precise and flexible IP framework that will provide incentives for participation from all sides of the research consortium ecosystem.

Major challenges in research consortia are related to effort synchronization, maintaining an open collaborative environment (due to IP leakage concerns among the members) and coordination between different consortium member’s needs. It is important to develop different modes of participation: full access membership, program-based with multiple participants, direct model with single company and/or incubator model to launch new companies. In addition, consortia work best when all parties have “skin in the game”. Members must be active participants and not just paid recipients of the output or funding. This includes active participation in technical direction setting and having member company assignee participants on the ground.

The governance model should be based on well-defined organizational structure with Board of Directors, Executive Steering Committee, Technical Advisory Council, and other committees/councils as needed, such as Program Management Office, IP Council, etc. with membership from industry, universities and government institutions. The Consortia structure needs to have ability to update the structure as the NSTC evolves.

To meet the goal of the NSTC, the governance and IP model need to be defined and articulated at the outset with constant/consistent/accurate communication with all parties to build a strong environment around trust and collaboration.

Below is a proposed governance model for NSTC. It should feature clear separation of roles duties for Oversight, Advisory, and Execution. The main governance model should ideally feature a tri-body system, with key responsibilities:

#### I. Board of Directors (Oversight)

- Define membership/participation requirements and fees
- Set Annual budget
- Provide strategic guidance and direction
- Appoint Executive Steering Committee members
- Charter and close BoD and ESC subcommittees as required

#### II. Executive Steering Committee

- Sets technical agenda with input from tech council
- Allocate program budget
- Manage member/participant assignee process
- Identify Technical Advisory Council members and Program Advisors
- Review Program Mgmt. Office performance

#### III. Technology Council (Advisory)

- Recommend technical agenda and roadmap
- Define technical programs and expected results

- Identify partner/network prototyping and manufacturing capabilities
- Recommend program budget allocations
- Select Industry and Academia representatives for Program Advisory groups

#### IV. Program Management Office (Execution)

- Executes on technical agenda and advise on project funding
- Manage shared facilities engagement
- Manage Program Advisory groups
- Review project performance

#### Question 9: Employee Assignments and Students

9. What attributes or capabilities of the NSTC would make it attractive and beneficial for companies, universities, and other agencies to want to send employees for assignments at the NSTC? What types of research and training opportunities should be made available at the NSTC for students and early career staff?

#### Response:

It is clear there is a real talent gap in the United States, not only in preparing the engineers, scientists, and coders of tomorrow, but also in training the future entrepreneurs that will ultimately be required to translate new semiconductor technologies from the lab to market. The NSTC & NAPMP should recognize this gap and proactively fill it by providing training, education, and professional development programs for people at all education and skill levels from K-12 through post-doctorate, with a focus on traditionally underserved populations of women, minorities, and veterans as well as relevant HBCUs, Minority Serving Institutions (MSIs), community colleges, and K-12 vocational programs throughout the country.

Key attributes and capabilities that NSTC should have to attract and make beneficial for companies, universities, and other agencies include: (1) access to state-of-the art (SOTA) facilities and equipment, (2) facilitated collaboration and networking opportunities, and (3) offer apprenticeships programs and jobs in government, academia, and industry. Supported by an open innovation ecosystem, exposure to new technologies, SOTA equipment and facilities would be a big draw for visiting researchers. The NSTC can be a force for the government, industry, academia to reduce the costs and risks associated with R&D and increase speed to market. The NSTC should build a better pathway for access to key facilities and equipment, collaboration amongst members, and the creation of jobs in the semiconductor industry that result in long-term outcomes for all Americans by.

- 1. Access to SOTA facilities and equipment:** NSTC participants want access to SOTA facilities and equipment to drive down cost and risk on R&D related activities. Access to centralized SOTA prototyping and design fabrication for building new devices and compute platforms using IP produced by these participants will attract and benefit organizations across the spectrum. Additionally, these facilities should provide test, debug, and demonstration capabilities, helping organizations achieve an accelerated path from R&D to commercialization. A shared NSTC facilities and equipment approach will provide access to domestic sources for advanced manufacturing to create functional prototypes for delivery against R&D activity with industry, academia, and national labs through various hubs and centers of excellence that provide design, manufacturing, materials, and other capabilities.
- 2. Facilitated collaboration and networking opportunities:** NSTC can build stronger ties between academia, industry, and government through facilitated opportunities that will enable organizations to collaborate with a wide spectrum of disciplines and skills across the microelectronics industry domain. Collaboration, open discussion, regular research presentations and reviews should be mainstays of the NSTC to ensure relevance and access to sharp minds and new ideas which will be paramount in advancing semiconductor technology. This provides organizations and individuals the ability to proactively address skills gaps and develop their skills for technology advancement not only in depth of knowledge but in breadth of knowledge. Supporting a workforce that will have the ability

to solve complex cross-discipline issues that challenge the microelectronics industry will attract new and experienced talent to well paid jobs already in the semiconductor industry.

**3. Offer apprenticeship programs and jobs in government, academia, and industry:**

Focus on partnerships between government, industry, and academia to create more STEM education opportunities as they relate to advanced semiconductor technology. Students and early career staff would benefit from seminars and hands-on training aligned with their degree programs from established professionals and subject matter experts with strong backgrounds in various semiconductor disciplines. Expanding STEM education offerings and skills-based credentials empowers learners and aligns their skills to in-demand apprenticeships and jobs. Expanding paid, hands-on learning for advanced careers in the semiconductor industry will attract both students and mid-career workers to the semiconductor industry and enables job growth.

The NSTC should also look to leverage national education efforts including K-12 focused STEM programs geared for training technology-based entrepreneurs like the National Science Foundation’s Innovation Corps (I-Corps) Program. There is a real opportunity for the NSTC to engage large swaths of prospective and serial entrepreneurs and start-ups in this space by plugging into select regional I-Corps locations around the country, some of which are also based at HBCUs and MSIs. The NSTC should prioritize solving the ongoing and growing training and workforce development mismatch between academia, industry, and the start-ups and smaller companies they engage with. If successful, this would address one of the most significant barriers to realizing a thriving domestic semiconductor ecosystem in the U.S.

**Question 10: NSTC Services and Processes**

**10.** For organizations that currently utilize an external semiconductor “fab” as part of their R&D efforts, what services or processes are currently missing in the U.S. ecosystem that the NSTC should provide?

**Response:**

The NSTC, through its hubs and Centers of Excellence, should provide broad access to semiconductor R&D and prototyping facilities across a range of technologies including leading-edge logic, memory, analog-mixed signal (AMS), radio frequency (RF) and power, to the entire U.S. semiconductor ecosystem. Today there are limitations, especially for small and medium sized companies, start-ups, and academia, to easily and cost effectively access these services and capabilities. In addition, there is no readily accessible domestic entry point for technology nodes beyond 14nm.

The NSTC can bring together EDA vendors, device designers, silicon manufacturers, tooling and material suppliers, and system developers to ensure end-to-end solutions. As a physical entity, NSTC should include access to state-of-the-art silicon process in a professionally maintained environment with a complete suite of advanced tooling to enable rapid cycles of learning on device architectures, interconnect schemes, new materials introduction, and novel design styles. The NSTC prototyping facilities should be positioned in close collaboration with the NAPMP Advanced Packing facilities, to ensure full stack systems-level optimization can be achieved, e.g., via heterogeneous integration.

The NSTC should provide broadly accessible leading-edge cloud-based EDA design capability, modeling, process design kits (PDKs), and intellectual property (IP) that are consistent with US leading- edge manufacturing capabilities, which will help ensure the successful transfer of prototypes to large scale manufacturing. A regular cadence of test vehicles and a multi-project wafer (MPW) strategy should be developed to allow facile access for content providers from across the spectrum of stakeholders.

Cycle times should be at industry competitive rates as measured in days-per-mask-level. This can be accomplished having multiple tools per process step and minimizing any one-of-a-kind process steps. Fab space should be dedicated to rapidly screen and integrate new materials, chemistries, and processes as needed. Coordination with imec for early access to high NA EUV and ancillary metrology as well as with participating OEM companies for early access to state-of-the-art tooling is essential. Opportunities for developing advanced machine learning for predictive yield-learning capabilities via digital twin approaches or other advanced AI approaches should be included.

**Question 10a:** Are there specific toolsets that the NSTC should own and operate or provide access to?

**Response:**

The NSTC will require full prototyping lines with state-of-the-art tools, including sufficient parallel paths (e.g., second-of-a-kind tooling) to ensure predictable and competitive cycle times to support its full mission. The lines will require full flow process tools, metrology, inspection, characterization, electrical test, failure analysis (FA), and packaging capabilities. Base infrastructure (slurry delivery, chemical, water supply, electricity, clean room, filtration, etc.) should be consistent with state-of-the-art foundry infrastructure. The lines should afford balance between discipline, to ensure stability and confidence in results, and flexibility, to enable rapid introduction and evaluation of new processes, materials and tooling. The NSTC should make a significant investment in resources and diagnostic capabilities to ensure that the defect densities are low enough to yield adequate numbers of functional devices. Sufficient metrology, inspection and failure analysis resources should be afforded to allow rigorous characterization without competition for baseline line management.

An initial, but not exhaustive, list of tools, processes, and services that NSTC should provide includes:

- 300mm development and prototyping lines with full equipment set capable of supporting multiple nodes for logic and generations of memory and other functionalities
- State-of-the-art lithography capability including extreme ultraviolet (EUV) scanner and access to high numerical aperture EUV tooling
- Centers of excellence facilities providing integrated processing to enable logic, memory, AMS, RF and power capabilities
- Advanced packaging capabilities in coordination with the NAPMP through co-located facilities where appropriate
- A 24-by-7 operation in the prototyping hubs with quality processes and methods and

competitive cycle times in line with standard operation to execute innovation and prototyping at speed with fast cycles of learning

- Comprehensive process controls and characterization (metrology, inspection & analysis capabilities) to enable prototyping and provide effective feedback on potential issues
- Advance fab controls in the prototyping hubs including statistical process control (SPC), fault-detection and classification (FDC), predictive maintenance, digital twins
- Complete device data, inline, metrology, test, failure analysis
- Baseline technology flows available for use including full design support ecosystem, PDK, and enablement support including a cloud-based shared EDA environment
- Protocols and logistical capabilities to enable wafer transfer between NSTC facilities and commercial fabs
- Additional space, flexible tooling, and resources to support novel material and process research and development
- Fab based tooling R&D with full commitment, and engagement of tool suppliers
- Leading edge capabilities, including beta tools for future technology generation innovation
- New material characterization for test that will not be accepted in standard foundries

### **Question 11: Start-up and Investment Fund**

**11.** As authorized, the NSTC could establish an investment fund, in partnership with the private sector, to support start-ups and collaborations between start-ups, academia, established companies, and new ventures, with the goal of commercializing innovations that contribute to the domestic semiconductor ecosystem, including advanced metrology and characterization for leading-edge manufacturing processes, and for security and supply chain verification. How should this investment fund be structured?



**Response:**

The NSTC should establish a hybrid approach to an investment fund while working in close partnership with the private sector to support semiconductor start-ups throughout the various stages of the commercialization lifecycle from lab-to-fab including (1) long-term investment horizon or patient funding, (2) access to highly specialized resources such as capital-intensive facilities and equipment, and (3) access to expertise and talent. As such, the NSTC's investment fund should be structured as a hybrid model to fill market gaps and accelerate the best semiconductor start-ups with both non-dilutive funding from grants and subsidies as well as dilutive funding from a professionally managed venture capital fund. This hybrid approach will bring the best start-ups to the NSTC which in turn will attract blue-chip, sophisticated financial and corporate investors with sizeable balance sheets that will be able to capitalize these start-ups through the several series of financing, and presumably tens or hundreds of millions of dollars, needed to achieve commercial scale and profitability.

**A. Non-dilutive funding through grants and subsidies to advance new discoveries from lab to early prototyping**

Non-dilutive federal funding programs, such as Small Business Innovation Research (SBIR), Small Business Technology Transfer (STTR), and Strategic Funding Increase and Tactical Funding Increase Program (STRATFI), are fundamental to bridge the gap between proof of concept and initial prototype. Traditional sources of funding, such as venture capital, typically require a certain level of technology de-risking and market validation, which can cost hundreds of thousands or millions of dollars, before they will invest in a start-up. In addition, access to prototyping facilities, tools, and equipment alone are very costly but are required to reduce technical and investment risk. As previously mentioned, the NSTC should provide access to shared facilities and bridge tools from its member organizations to participating start-ups, so those start-ups are as capital efficient as possible and do not have to deploy investment capital to purchase and operate new prototyping facilities and equipment that already exist.

**B. Venture capital model to support scaling and growth of early-stage start-ups**

The venture capital fund component of NSTC's investment fund should be structured as a

limited partnership between government, member organizations, and the investment community. It should follow the proven models of leading blue chip venture capital and top-tier corporate venture capital firms that invest in hard-tech start-ups developing long-term horizon technologies (e.g., In-Q-Tel, The Engine, Applied Ventures, etc.). In this structure, there should be: (1) a General Partner who operates the fund and manages the partnerships; and (2) one or more Limited Partners who supply the investment and operating capital for the fund(s).

The General Partner should be responsible for capitalization efforts, operations, management of partnerships, selecting investment targets, and managing the portfolio of investments to exit. As such, it requires a management team with strong understanding and connections within the broader industry, deep insights regarding technology trends and innovation in the semiconductor space as well as experience with early-stage investments. The General Partner, in collaboration with the government, Limited Partner(s), and any other relevant parties, may define the investment thesis for the NSTC venture capital fund around certain technology themes or stages of development. For example, the investment fund may require matching funding from other investors, or it could be a fund that preserves the ability to lead deals for more flexibility in deploying capital.

The Limited Partner(s) would commit capital to support the life of the fund (typically set at 10 years) and can have some high-level oversight through an advisory board role as outlined in the Limited Partner Agreement. Limited Partner(s) do not have direct or day-to-day control other than the ability to replace the General Partner if ever needed.

**Question 11a:** What should be the roles of the public and private sectors in capitalizing, operating and overseeing the fund and selecting its investment targets?

**Response:**

We envision the public sector capitalizing, operating, and overseeing the non-dilutive grant funding and subsidy programs – similar to the existing programs mentioned above (SBIR, STTR, and STRATFI). It is imperative these non-dilutive programs offered by the NSTC for

earlier stage opportunities can provide supplemental matching funds for start-ups that gain traction with investors or strategic partners. These types of matching funds programs, which the NSTC could replicate relatively easily, are highly effective in attracting private capital from investors alongside the federal dollars while also unlocking additional valuable non-dilutive funding for the recipient company's continued development and growth.

For the venture capital fund, we envision the government partnering with industry to set up an independent fund that supports the mission of the NSTC, investing in early-stage start-ups (seed through Series B), providing portfolio companies access to critical resources, and facilitating relationships with the broader industry and government agencies. The NSTC's venture capital fund should be structured in a way such that any returns or proceeds from the government's or partner organizations' share of the overall fund can be reinvested in future venture capital funds or reinvested in other programming.

**Question 11b:** Should the investment fund focus on early-stage investing, late-stage investing, or other stages of the process?

**Response:**

With the primary goal of bringing breakthrough technologies to market, we recommend that the investment fund focus on patient, early-stage investing, which is where the primary market gap resides. This includes seed to Series B financing stages to support start-ups past the development phase and into market introduction, in addition to pre-seed stage non-dilutive grants and matching funds such as the ones mentioned above. Once a technology is demonstrated to be viable by prototyping in the NSTC, and a sound business plan and team are in place, funds for scaling up should be obtained from traditional sources such as later stage venture capital, private equity, strategic investors, and customers.

To help drive more success at the risky early stages, investments in start-ups should be complemented with an incubator model and related commercialization support to provide:

## American Semiconductor Innovation Coalition (ASIC)

- Access to shared facilities, tools, and equipment required for design, development, proof of concept, and prototyping
- Industry expertise to help validate ideas from concept to prototyping as well as integration with the broader ecosystem and supply chain
- Access to market and customers
- Business and commercialization mentorship
- Entrepreneurial education and training for both business and technical roles

Typically, successful investors provide more than just capital, they also provide added benefits such as the ones listed above. Therefore, the selection of a General Partner and Limited Partners should be an important consideration when creating the NSTC's venture capital fund vehicle.

**Question 11c:** How should the fund interact with existing private capital, both venture capital and established investment capital?

### **Response:**

The Fund should look to establish or leverage existing strong working relationships with other experienced venture capital funds and corporate investors as co-investors. These firms already have a track record of establishing and sustaining venture funds, screening companies and performing diligence, and helping early-stage portfolio companies scale quickly. This collaboration also allows for buy-in from multiple ecosystem stakeholders simultaneously and provides risk sharing at this critical stage for start-ups.

As such, the NSTC investment fund should be actively promoted to and closely aligned with venture capital and growth capital sources needed by both the start-ups and industry it serves. Non-dilutive grants and matching funds should be marketed effectively to investors and other development partners to promote follow-on funding to start-ups. Venture capital investors would look to take advantage of the matching funds for earlier stage companies while the growth capital

investors would look for investment and other business opportunities with the later stage companies supported by the NSTC that are reaching the market. This mutually beneficial cycle of the NSTC de-risking prospective investments for the investment community and those investors then putting more capital into the start-ups and smaller companies supported by the NSTC would create ample opportunities for these groups to continue to interact and work together.

One approach for ensuring the NSTC interacts with private capital sources is to utilize the organization's advisory body, or a focused subset of it, to oversee and weigh in on the activities of the investment fund program or other topics of particular importance to the organization. In this scenario, the NSTC should engage a diverse and inclusive mix of representatives from the full spectrum of capital providers (government, philanthropic, angel, venture, corporate, growth) that are available to semiconductor start-ups. Consistent and thoughtful engagement of these industry partners will ensure the NSTC, its investment fund, and the companies its supports remain close to the market.

**Question 11d:** How can the fund sustain itself through its investments?

**Response:**

As mentioned above, we envision a hybrid investment fund model with both non-dilutive grants and subsidies for earlier stage opportunities as well as dilutive venture capital investment for start-ups that successfully scale from prototype to fab with the NSTC's support. The NSTC venture capital fund portion could be structured as "evergreen" based on successful exits from earlier investments. In this scenario, the NSTC's venture capital fund would be structured in a way such that any returns or proceeds from the government's or partner organizations' share of the overall fund can be reinvested in future venture capital funds or reinvested in other relevant programming. A venture capital fund typically expects a successful exit of 1 out of every 10 investments, taking at least 5 to 10 years to begin generating meaningful returns from exits on the initial investments made in early years. Deep tech such as semiconductors will be on the longer end of this range.

It is imperative to emphasize that the terms of a dilutive round of funding should not adversely affect the recipient companies' ability to secure additional capital from future investors given their

stage of development. Often start-ups and smaller companies in this space are expected to accept terms for early financial or development support that would make it nearly impossible for them to raise follow-on capital down the line so the NSTC should be mindful of that in how it operates.

### Question 12: International Partnership

12. How should the NSTC's investments and focus overlap or complement the investments and capabilities of foreign institutions such as the Interuniversity Microelectronics Center (imec) in Belgium or the French Laboratoire d'électronique des technologies de l'information (CEA-Leti)?

#### Response:

Many U.S. based companies have long standing relationship with foreign institutions in Europe or Asia. Also, some key technology enablers are not and will not be developed in the United States, making the collaboration with foreign institutions a requirement. In all cases, a full overlap will not make sense for cost and resources reasons. We recommend developing a foreign institutions collaboration with the following principles.

- Collaboration with foreign institutions which are not established within “foreign entities of concern”, as defined in the 2021 National Defense Authorization Act, should be supported for research and development. If performed abroad, through the partnership within the NSTC, focus on technology agenda elements should be funneling pre-competitive elements or complementary work. In all cases, prototyping should be performed on U.S. soil.
- When required to execute the NSTC agenda, collaboration with foreign institutions could be done at a foreign site or at U.S. based centers with resources allocated from foreign institutions in U.S. or U.S. assignees in foreign institutions. This will enable cross learning and skill upgrade for all NSTC participants.
- When specific and unique capabilities exist in the United States or abroad, a two-way partnership should support access to these mutual capabilities and should be provided to create

a win-win for the participants and hence advance the NSTC programs. Many similar programs are underway in many parts of the world (EU, Japan, Korea). We recommend the government sponsors for all sides to promote and enable cost sharing and capex optimization across continents, as well as accelerated technology availability and international collaboration.

- NSTC should propose an exchange program at both the student and senior technical level to enhance cross-learning and workforce skill development as well as to foster collaboration.
- A key concern will be the control of the IP and technology being developed within the NSTC and potential availability to non-authorized foreign countries. We recommend that foreign institutions must set dedicated and controlled “fire walls” between NSTC and U.S. interests, specific programs and all other activities.
- We also recommend that foreign research institutions, strategically participating in NSTC, in the United States or abroad, may not be granted voting governance roles or strategic management positions within the NSTC infrastructure, but true partnership will require representation in strategic boards and road mapping bodies.
- As a first order of priority, we recommend bringing the coordinated strategic value of a partnership with imec in the NSTC for screening technology options 3 to 4 generations ahead of manufacturing on advanced CMOS, memory, 3D integration, and analog derivative technologies etc. for early access to high NA EUV and ancillary metrology. A strong partnership within NSTC with the appropriate IP models will help to advance NSTC capabilities and accelerate success of the collaborative effort of the network. It will not be efficient to try duplicating imec’s work but leveraging expertise and capabilities by involving imec will be most effective and in the benefit of NSTC.

Subject to government approval, we also recommend participation of foreign OEM companies for early access to state-of-the-art tooling. As an example, together with ASML, a joint High-NA EUV Lab imec (HQ in Belgium) is focusing on the infrastructure preparation which is necessary for high-NA scanner development.

## ADVANCED PACKAGING

### Question 1: Long-term National Leadership

1. Please describe the application areas that are essential to long-term national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs. Examples include but are not limited to:

- Analog device packaging
- Automotive
- Defense and aerospace
- Energy generation, transmission, conversion, and storage
- Harsh environments
- High performance computing, quantum computing, data centers
- Integrated photonics
- Integrated power electronics
- Internet of Things
- Mature packaging
- Medical, health & wearables
- MEMS and sensor electronics
- Mobile telecommunications
- Other



**Response:**

The primary applications driving much of today's advanced packaging technology development are advanced compute, advanced wired and wireless communications, automotive, and edge devices (including IoT and wearables). The specific details of each of these are explained in the following paragraphs, followed by some of the key technologies that will be critical to enable advances in these application spaces.

**1. Advanced Compute: High Performance Computing (HPC), Artificial Intelligence/Machine Learning (AI/ML), Virtual/Augmented Reality (VR/AR), Gaming, Blockchain technology, Crypto-mining, and some Aerospace and Defense (A&D)**

These compute-intensive applications require access to significant amounts of memory. Improvement in logic-memory bandwidth is paramount. This is an application where there is an important trend towards chiplet-based architectures. A "chiplet" is an integrated circuit block specifically designed to work with other chiplets to form a larger more complex system that often makes use of reusable IP blocks. Ensuring adequate, high-speed bandwidth across the chiplet interconnections presents an important packaging challenge. This trend towards chiplets is an opportunity for the nation to regain leadership in packaging and heterogenous integration. Technologies that enable low-latency interfaces to disaggregate shared memory (physically separated from the logic) will unlock significant performance and efficiency improvements in advanced computing environments. Thermal, reliability, and manufacturing yield considerations are also important here.

These applications have a large carbon footprint and so there are two critical factors: 1) Memory – compute interaction optimization based on application and 2) Sustainability – especially for data intensive workloads like AI/ML, where compute / power efficiency must be a priority, as current trends in computational needs and corresponding power consumption is not sustainable. The data explosion generated by the growth in social networks and digital entertainment, cloud-computing, and IoT are radically driving the growth of data centers and the need for high bandwidth, low-latency, and low power consumption communications. 2.5 / 3D and silicon photonics are 2 technologies that can address this application need as traditional packaging technologies are becoming input/output (I/O) limited so there is a trend towards

these new interconnect paradigms. The generational progression drives tighter integration between network switching and optical I/O that will probably culminate with 3D co-packaged optics with integrated lasers on chip. Co-packaging of electronics and photonics with heterogeneous integration of lasers with silicon photonics is the current focus. Higher bandwidths are needed, and the current roadmap depends on integration of electronics and photonics<sup>8</sup>.

## 2. Advanced Communications (Wired and Wireless)

- **Wired (Server/Switches/Routers):** These applications form the backbone of modern communications infrastructure and the underlying packaging competencies revolving around large form factors. High density organic substrate-based flip chip packaging and wafer level packaging should be a leadership objective of the U.S., in addition to new package materials and paradigms. As scaling has slowed, the drive should be toward high radix-chiplet based switches to achieve 100Tb/s. Co-packaged optics including silicon photonics, light source (lasers) with optical interfaces (fiber, wave guide, couplers or other) are emerging as higher bandwidths and lower power are needed. Interface speeds will trend towards 100GHz and beyond which requires heterogeneous integration for front-end electronics such as III-V semiconductors in addition to CMOS technologies. The potential for dielectric wave guide communications interfaces should be comprehended as well.
- **Wireless (Smartphones/IoT):** Approximately 1.5B smartphones and a corresponding volume of IoT devices are sold each year and they are a necessity for modern life. These pervasive devices have specific packaging needs focused on cost and small form-factor, which requires massive scale in manufacturing and ultra-low labor costs. These applications require need to address a wide range of frequencies and extreme integration for small form factor and power efficiency. With pervasive connectivity and autonomous mobility expected in the near future, the need for supporting mmWave frequencies into the sub-Terahertz frequency range that includes 5G and 6G technologies becomes necessary. RF modules need to therefore support both infrastructure and handset requirements that

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<sup>8</sup> Margalit, Xiang, Bowers, Bjorlin, Blum, and Bowers, “Perspective on the Future of Silicon Photonics and Electronics”, Applied Physics Letters Perspective, (2021), and IPSR Roadmap Datacom

include integration of antenna in package (AiP), embedded electronics near the antenna arrays, robust heat removal methods, support for ultra-thin form factors, integration of advanced low loss and low dielectric constant materials, and others.

### **3. Automotive Advanced Driver Assistance Systems (ADAS) / Electric Vehicles (EV) / Infotainment)**

Semiconductor supply chain issues have most prominently been seen impacting the automotive industry. There are several important underlying packaging technologies that will continue to enable innovations in driver automation and vehicle electrification including those mentioned in Advanced Compute above to enable AI for ADAS, which also requires advanced System in Package (SIP) for sensor fusion. EV drives packaging needs related to power electronics and are driving packaging and advanced system in package (SIP) developments as well. Harsh environment considerations dominate “under-hood” applications and have important packaging implications.

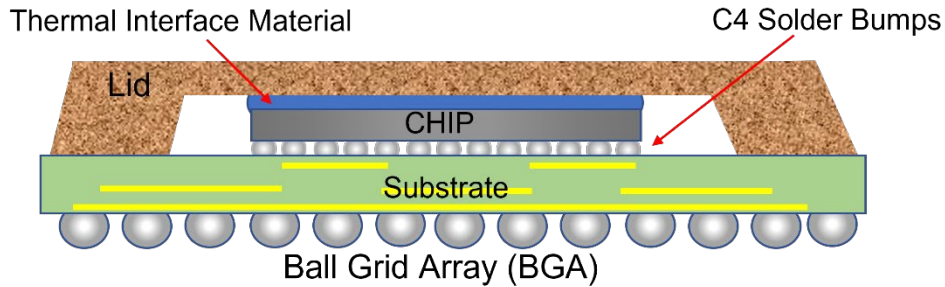
### **4. Edge Devices (including IoT and wearable)**

The proliferation of edge devices includes smart devices (IoT) for consumer, industrial and defense. These edge devices address new applications in many areas including for example Health, Medical, Wearables and Harsh Environments which are a key driver of new packaging technologies.

The packaging platforms to support these applications should focus on the following core technology elements:

#### **a) FLIP CHIP (FC)**

Flip Chip technology has grown very rapidly from the days when it was introduced by IBM through its classic C4 (controlled collapse chip connection) technology in the 1980s, and today is a mainstream choice for semiconductor packaging.



**Figure 1: Cross sectional illustration of a flip chip package.**

Source: Courtesy of IBM

FC packages are fabricated with the silicon functional die directly connected to the substrate with a solder bump array as shown in Figure 1.

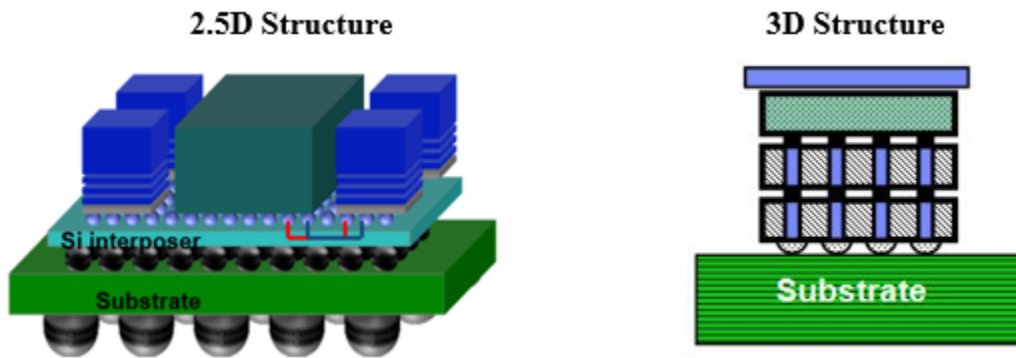
**b) Fan-out Wafer Level Packaging (FO-WLP)**

Logic-memory integration sought after in many high-performance compute-related applications continues to drive fan-out packaging using known-good-die (KGD) to reconstitute a wafer and then perform interconnect steps through redistribution layers (RDL) using semiconductor grade equipment for higher interconnect densities than otherwise possible with conventional organic substrates. There are a wide variety of technologies here and a great deal of background IP to navigate; however, this is a critical technology for the future of packaging.

There are two broad categories of FO-WLP: low density (LDFO) and high density (HDFO), which alludes to their wiring densities. LDFO is typically used for smaller die and with lower IO count and RF applications and forms the entire package structure. HDFO is used in the general case for multi-die integration requiring sub-5 um signal line widths and spaces and is generally used to create a sub module which is then attached to the organic substrate to complete the package structure. In addition, there are different manufacturing processes with again two broad differentiators: Those that commit the silicon die to the package prior to creation of the RDL (redistribution layer) wiring (“die first”), and those that create the RDL first and then attach the KGD (“die last”). The U.S. should strive for leadership in “die last” related technologies as opposed to already prevalent “die first” approaches.

### c) 2.5D Module-Level Integration and 3D Integration

3D type packaging is practiced in high volume in the DRAM space to create High Bandwidth Memory (HBM) stacks used in memory intensive compute activities like gaming and AI/ML. In many cases silicon die cannot be interconnected using a FC substrate, due to the fine-line signal routing density required between the die. When this occurs, a higher-density signal routing solution is required. There are two primary paths: (1) 2.5D integration using silicon, glass or organic interposers, with multiple functional die positioned closely together on the interposer and the interposer providing fine pitch wiring and bond pads for 2D interconnection of the die as shown in Figure 2. (2) 3D integration, with multiple functional die stacked vertically as shown in Figure 2 as well. The next evolution of 3D is the integration of logic and memory die (e.g., Intel’s Foveros process and AMD’s 3D VCache).



**Figure 2: Cross section illustration of 2.5D and 3D packages**

Silicon interposers require a silicon fab backend process, which limits the availability for this packaging sub-component. This limitation can place a stranglehold on specific packaging options in this space and in general stifles competition and innovation. HDFO, which is also an interposer technology, is more generally available although still a relatively new technology offering and replaces the inorganic dielectrics with organic dielectrics as well as options for silicon bridge technologies. Limitations on a given provider’s capability to perform all necessary steps including Thru Silicon Via (TSV) insertion fine pitch redistribution layers (RDL) and fine pitch solder bumping, as well as lack of interest/business case in providing cost-effective silicon interposers as a standalone commodity item (relative to that silicon going towards active devices) are both roadblocks that need to be addressed.

3-D should be explored in chiplet form with both compute on top and memory on top configurations. Die stacking can be achieved using current soldering methods and this will suffice for some product classes. However, for the next decade the ability to stack die of different foundry origins and different sizes using hybrid bonding technology with no solder bumps and tens of thousands of interconnects per square millimeter will provide a true breakthrough in performance and lower power. Ultimately, 2.5D and 3D and combinations of each should be explored for both chiplet combinations, and chiplets plus DRAM memory stacking.

Finally, it is important to note that HDFO interposers are also gaining market acceptance, especially for the integration of multiple chiplets with high-speed die to die interfaces. We believe that this is an area where future leadership is critical to the United States and, therefore, should be prioritized for funding.

#### **d) Advanced Memory (FLASH/DRAM)**

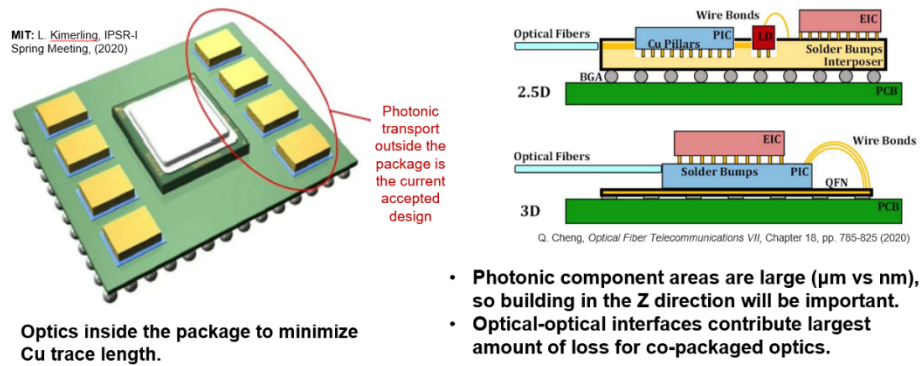
All modern electronics applications require memory, both volatile (DRAM dominated) and non-volatile (FLASH dominated). Each of these critical memory applications have their own unique packaging needs:

- FLASH: Advanced wirebond technology
- DRAM: Wirebond dominated, with increasing use of flip chip and 3D technologies particularly for high bandwidth memory (HBM) applications

Note that High Bandwidth Memories are driving 3D interconnect technology, now at micro-bump scale and hybrid bonding on the horizon.

### e) Silicon Photonics

Achieving ultra-high data transmission rates may require moving to integrated photonics technologies for some applications; early versions are already prevalent for data center applications and will become increasingly important in communications, life sciences, A&D, and other sectors. These applications require integration of photonics ICs with high-bandwidth memories, traditional CMOS and analog ICs, and integrated lasers, all requiring advanced packaging techniques (see Figure 3).



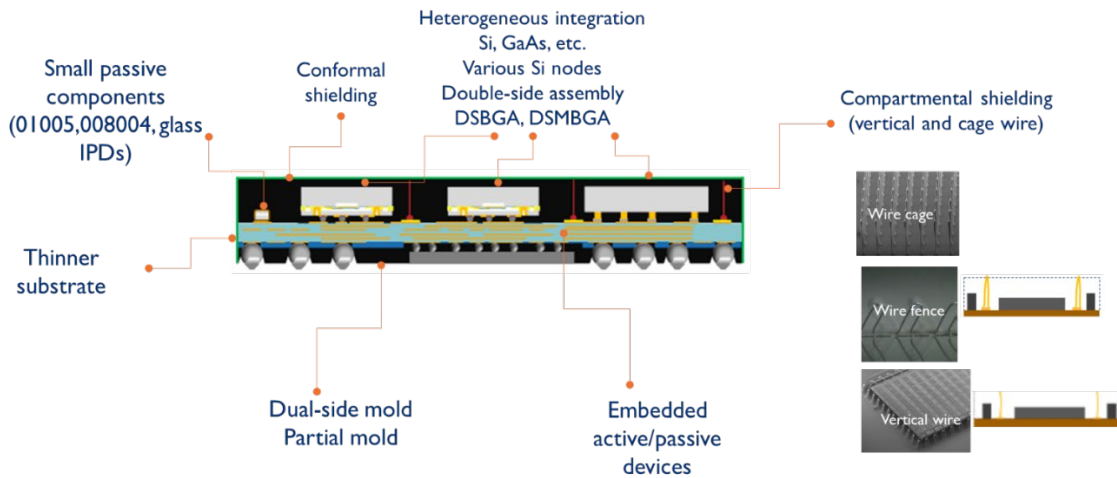
***Innovation in vertical optical interconnects will enable scalable CPO.***  
**Figure 3: 2.5/3D innovations for co-packaged optics (CPO)**

### f) High-Reliability / Harsh Environments

There is increasing overlap between commercial applications (such as automotive) and A&D needs for high-reliability packaging for harsh environment applications. Advanced packaging techniques that are highly reliable across wide temperature ranges, shock and vibration, radiation, etc. while still preserving a long operating and storage life are of critical importance to the U.S. commercial and defense industrial base. The diversity and complexity of advanced packaging manufacturing technologies means that many of the current state-of-the-art techniques have not yet been optimized or qualified to survive under these conditions. While the market sector requiring high reliability may not be a major driver of volume production, ensuring domestic leadership in this space is critical to ensuring that the automotive and defense industries are able to adopt these advanced technologies in the national interest. Radiation hardening can be important in A&D applications and should be considered as well. Vibration needs to be studied for high reliability photonic integration.

**g) System-in-Package (SIP)**

Many consumer and wireless communications applications require that the SIP configuration be manufacturable in high volumes at very low cost. RF Front-end (RFFE) modules for smartphones provide an excellent example of SIP technology. Some edge applications benefit from the integration of many (often hundreds) of disparate components such as compute, memory, analog or mixed signal, discrete, and/or sensors frequently in a double-sided configuration to create a functional sub-system in a very constrained space (see Figure 4). Additionally, the A&D sector looks to readily leverage SIP-style packaging for RF, digital, and other technology needs; domestic, state-of-the-art capabilities in this area are essential to service these industries. Specifically, microelectromechanical systems (MEMS), sensors, passive devices, and filters, as well as multiple semiconductor technologies, such as SiGe, GaAs, GaN (III-V technologies) with CMOS with frequencies ranging from sub-1GHz towards greater than 100GHz will need to be addressed. SIP can take on various forms including flip-chip on substrate or interposer, wafer bonding, embedded die/components, die-on-die, stacked devices (TSV or bonded) among other approaches.



**Figure 4: SIP Example: 5G RF Package Technology Toolbox**

*Source: Yole Development System in Package 2021 Report*

Table 1 below summarizes the application of different packaging technology to various device types to service a broad range of end applications. The packaging technologies highlighted in



red are important for the NAPMP to focus on to establish broad technology leadership to service critical end use applications.

**Table 1: Packaging technologies to enable a broad spectrum of devices across multiple applications**

		DEVICE TYPES								
		CPU/GPU /APU	MCU	ASIC	FPGA	FLASH	DRAM	Analog/ Discretes	Sensors	Opto-electronics
APPLICATION	HPC				FC FOWLP					2.5D/3D, FC, SIP, WB
	AI/ML			FC FOWLP	2.5D/3D		WB, FC, 3D			
	Blockchain/	FC								
	Crypto	FOWLP		2.5D/3D						
	AR/VR	2.5D/3D				WB	WB		FC, WB, FOWLP, SIP	
	ADAS/EV		FC, WB				3D			
	5G/6G			FC			WB			
	Mobile						FC		FC, WB, FOWLP, SIP	2.5D/3D, FC, SIP, WB
	IoT		FC, WB				WB		SIP	
	A&D	FC, FOWLP, 2.5D/3D						SIP, FC, 2.5D/3D, FO		

**Key: Flip Chip (FC), Fan-Out Wafer-Level Packaging (FOWLP), 2.5D/3D, Wire Bond (WB), System in a Package (SIP)**

Source: Adapted from Yole Development

It is important to recognize that each of the packaging focus areas will need to develop specific test methodologies and test capabilities. These capabilities should be located within the packaging hubs they support.

**GROUPINGS**

Creation of a Si and Packaging Integration Center focused on an Open Chiplet-based

Ecosystem would be very beneficial and should be co-located with the appropriate NSTC Hub. Packaging technologies with a fundamental dependency on wafer level processing such as FO-WLP, 2.5D and 3D can be, and should be, grouped together in one hub. These technologies are also best co-located with an advanced silicon R&D facility where synergies in tool sets, infrastructure, and personnel exist to tackle interrelationships between the semiconductor and packaging technologies.

Packaging technologies that do not have a fundamental dependency on wafer processing can be pursued at independent pilot lines. At a minimum, pilot lines should be able to fabricate prototype packages in a manufacturing relevant tool set. They must include flip chip packaging, organic and glass substrates, advanced SIP, photonics, and flexible electronics capability. These technologies are critical to support the advanced packaging domestic need and landscape; however, they are not required to be as closely or inherently linked to a semiconductor fabrication facility to be integrated into the ecosystem. As such, hubs for these technologies can leverage and mature existing domestic supplier capabilities under the guidance of the NAPMP/NSTC centers and partners.

## Question 2: R&D Core Competencies

2. Please describe the R&D core-competencies that are essential to national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs. Examples include but are not limited to:

- Alternative materials to mitigate impact of supply chain disruptions
- Artificial intelligence for design of packaging
- Assembly and test
- Emerging materials
- Heterogeneous integration, chip stacking, and related technologies.

- High-density substrates
- Metrology
- Modeling and simulation
- Package-level design/codesign tools for electrical, thermal and mechanical design of complex packages
- Printed circuit boards
- Safety and security
- Software, firmware, new concepts in programming
- Standards
- Test solutions to assure yield in complex packages
- Thermal solutions for multi-die packages
- Tooling
- Other

**Response:**

The four seminal packaging platforms highlighted in our response to question one (Q1) (FC, FO, 2.5D/3D, SIP) require a common set of core competencies as well as some unique competencies for each platform. Table 2 summarizes the required core competencies by packaging technology platform.

**Table 2: Core Competencies by Packaging Technology Platform**

	FLIP CHIP	FAN-OUT	2.5D/3D	SIP	Comments
Semiconductor-Packaging Co-design					Especially important for 2.5D/3D
AI for Design					For improved layout efficiency and electrical performance
Modeling and Simulation					Broadly required
High Density Substrates					FO and 2.5D/3D take pressure off of the substrate technology
AI for Process Control					For improved yield and thruput
Advanced Materials					Broadly required
Wafer level processing					Need bumping for Flip Chip
Fine pitch assembly					Broadly required
Innovative Litho					Big opportunity for wafer level process related technologies
Inline Inspection & Metrology					Required for AI for process control
Advanced Thermal Solutions					Varies widely by end application
Photonics co-packaging					Emerging technology for high bandwidth applications
Wafer and Module Test					Critical for any new technology
Characterization & Reliability Testing					Critical for any new technology

Very low level of need in most cases    Very high level of need in most cases

While each packaging platform has specific core competencies of high importance, design, modeling, analysis, and simulation are critical in all platforms. For example, tools with AI capabilities are needed to enable advances in semiconductor--package co-design, 3D design, as well as thermal, mechanical, electrical, and photonic modeling of new architectures, and model-based predictions for reliability mechanisms and failure modes as well as hardware verification of these models. Non-traditional imaging approaches may be required for scaling primarily for wafer related packaging technologies. Standards for interfaces and interconnects will facilitate chiplet designs that can be used flexibly across different packaging platforms. New test methodologies and solutions will be required, some of which will be application specific. Of note, Known Good Die (KGD) solutions, especially detecting potential electrostatic damage (ESD) prior to assembly, enabled through test will be critical for multi-chip module and heterogeneous integration / chiplet applications to ensure adequate cumulative yield along with appropriate module level test solutions

that incorporate workload based functional test capabilities, particularly for High Performance Computing (HPC) and other high-end applications. Redundancy solutions will also be needed in most approaches as advanced packaging constructs are not easily amenable to rework. Similarly invoking redundancy and repair options post burn-in and in the field will be mandatory.

AI driven process control enabled by inline inspection, metrology and advanced process control (APC) techniques presents an opportunity to improve yields and process throughputs across all packaging technologies. As the industry trends towards fine pitch interconnects and assembly, this will be an opportunity for the U.S. to gain a technology leadership position.

Organic high-density substrates are used extensively across the microelectronics industry, due to their combination of high routing density (relative to conventional printed wiring boards), high production maturity, low cost, and large panelized production formats. While technologies such as fan-out wafer-level packaging (FO-WLP) offer alternatives for certain applications, high density organic package substrates will remain critical to the microelectronics industry. The supply base for these substrates and the laminate build-up materials that comprise them is, at present, entirely offshore and concentrated in Southeast Asia. With the recent rise in consumer microelectronics demand, the package substrate supply chain (both raw materials and fabrication) is massively constrained and has caught media attention just behind the chip shortage as a whole. Onshore capability to meet this critical need for the domestic commercial, automotive, and the A&D sectors must be a critical priority addressed by the NAPMP. Effort should be targeted at addressing the feature size, layer count, and capacity targets required across the various industry users and applications, while also addressing R&D in new, state-of-the-art laminate materials and processes to pioneer the next generation of domestic package substrate offerings. The existing domestic network of conventional Printed Circuit Board (PCB) manufacturers can function as a base from which this capability can be created. By leveraging the NAPMP's other hubs as users/customers, the NAPMP will drive technology needs and business cases for transformational investment in the domestic supply base.

Hardware security and provenance are critical competencies that should be developed to guard against counterfeit components and tampered devices which contain eavesdropping circuits to facilitate side channel attacks. This includes both design and IP data security to prevent inclusion

of eavesdropping circuits as well as technologies to uncover vulnerabilities should they occur. A multiphysics simulation platform enables electrical, electromagnetic, and thermal emission signatures to be captured for large sets of data. This can be analyzed to assess vulnerability to data or IP leakage via physical side-channels. Similarly, these emission signatures can be used to detect anomalies from silicon measurements. Provenance involves developing measurable security practices across the supply chain for heterogeneous systems.

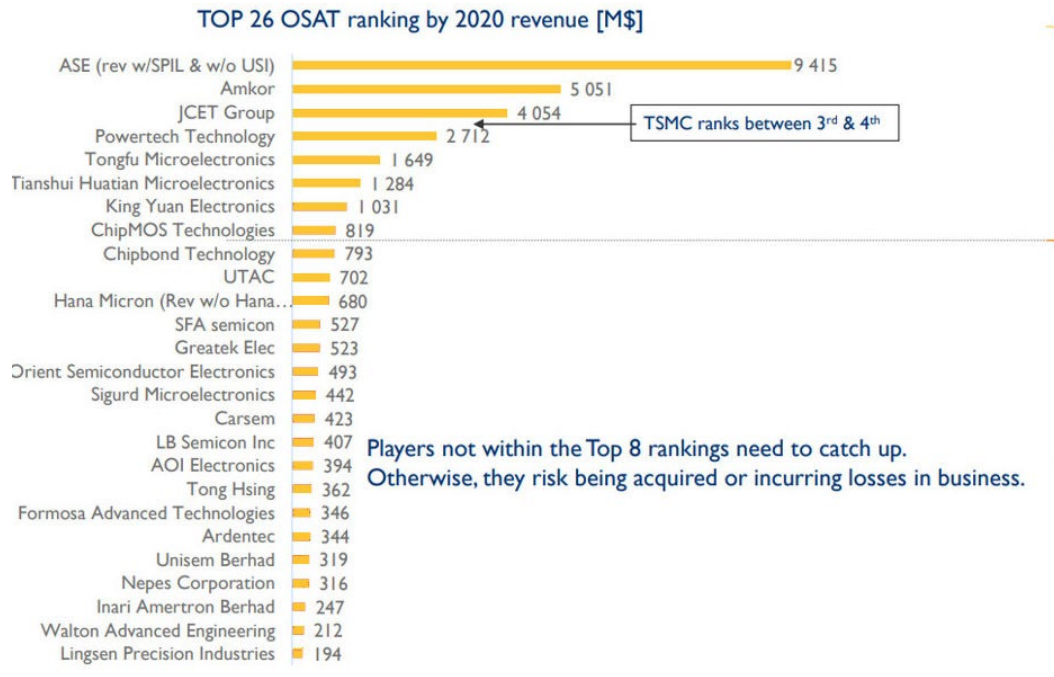
### Question 3: Diverse Needs

3. The proposed National Advanced Packaging Manufacturing Program (NAPMP) could be oriented to address multiple needs, including but not limited to prototyping, the provision of pilot lines, work force development, and supply chain development. Please describe the most critical needs on which the program should focus.

#### Response:

There are critical gaps in the U.S. domestic packaging capability and self-sustainment. An appropriate prioritization would be:

1. **SUPPLY CHAIN DEVELOPMENT:** There are significant gaps in the packaging supply chain including domestic materials, equipment, and organic substrate suppliers as well as a lack of domestic Outsourced Semiconductor Assembly and Test (OSAT) capability. Without correction here, there is no path to any level of self-sufficiency.
  - **OSAT Capability** is largely based in Asia, with only one of the top 20 OSATs being headquartered in the United States and even that one (AMKOR) has no U.S.-based manufacturing (see Figure 5). There are a small number of niche OSAT services in the U.S.

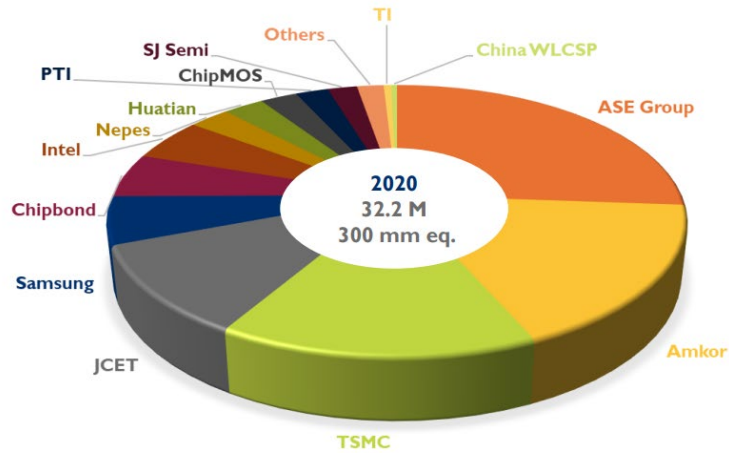


**Figure 5: Top OSAT Ranking by 2020 Revenue**

Source: Yole Development, *Status of the Advanced Packaging Industry, 2021*

This poses a significant problem since OSATs package most of the global output of advanced silicon wafers. A total of nine companies including one Foundry (TSMC), six OSATs (ASE Group, AMKOR, JCET, PTI, Nepes, and Chipbond) and two IDMs (Samsung and Intel) package 75% of the global output of advanced silicon wafers (see Figure 6). This is an important factor when considering who will scale up the technology output of the NAPMP for domestic manufacturing capability.

### 2020 ADVANCED PACKAGING WAFER SPLIT (300MM EQ WSPY)

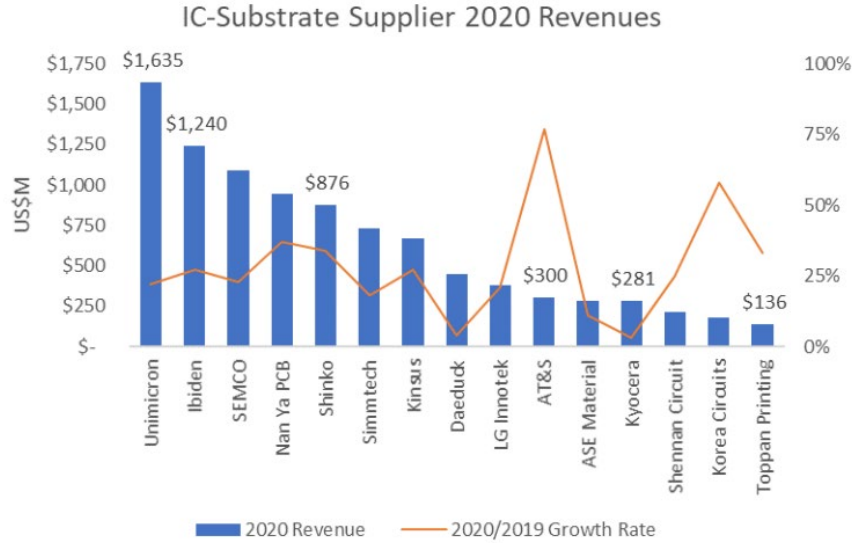


**Figure 6: 2020 Advanced Packaging Wafer Split (300M EQ WSPY)**

*Source: Yole Development, Status of the Advanced Packaging Industry, 2021.*

- **Organic substrates** are foundational to all advanced semiconductor applications today. This includes both Flip Chip (FC) substrates as well as PCBs for second level packaging. These components are manufactured almost exclusively in Asia (most of it in China/Taiwan). The recent IPC report has important further details, and the reader is encouraged to review that report in its entirety (IPC Industry Report “North American Advanced Packaging Ecosystem Gap Assessment, Nov 2021). Figure 7 below from the IPC report shows the top 15 IC substrate suppliers globally. None are U.S. companies or have any U.S. based production. However, the existing domestic network of conventional Printed Circuit Board (PCB) manufacturers can function as an existing base from which to create this capability, potentially across multiple suppliers. By leveraging the NAPMP’s other hubs as users/customers, the NAPMP will drive technology needs and business cases for transformational investment in the domestic supply base.





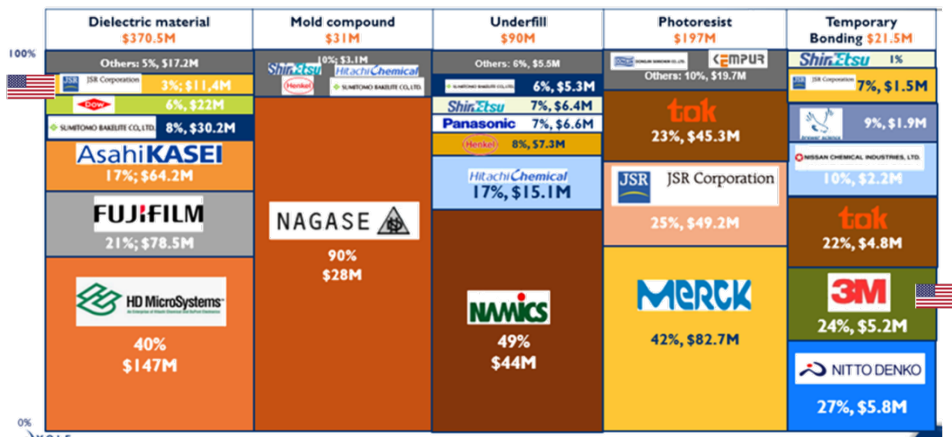
**Figure 7: IC-Substrate Supplier 2020 Revenues**

Source: IPC Industry Report “North American Advanced Packaging Ecosystem Gap Assessment, Nov 2021

- Advanced Materials:** Execution of any packaging technology requires an array of specialty materials for both the interconnect fabric (e.g., organic dielectrics, photoresists, and copper) as well as the assembly process, which includes underfills, solders, gold/copper/silver wire, thermal interface materials, molding compounds, adhesives, and encapsulants to name a few. The vast majority of these are produced outside of the U.S. by companies headquartered outside of the U.S. (see Figure 8).

**2017 POLYMERIC MATERIALS MARKET SHARE - WORLDWIDE**

In the field of Advanced Packaging



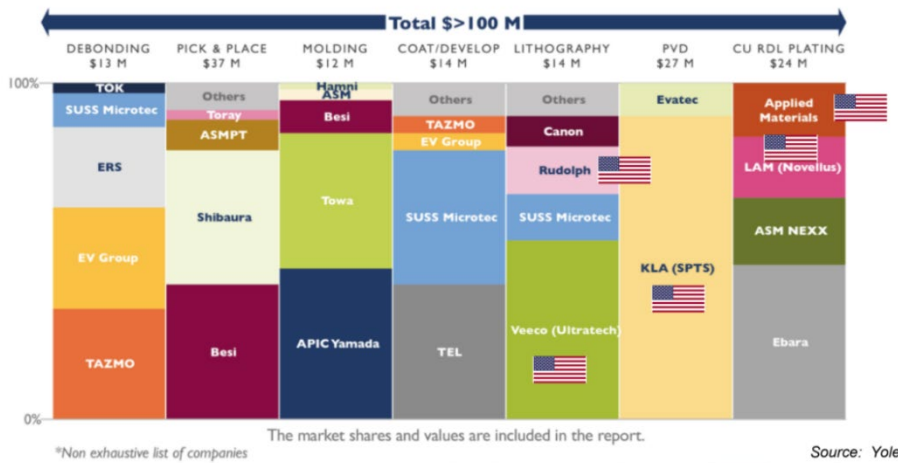
**Figure 8: 2017 Polymeric Materials Market Share - Worldwide**

Source: Yole Development

While there are some U.S.-based packaging equipment companies, much of their production is in Asia, and then many other key companies are headquartered in Asia as well (e.g., ASM-PT). This dependency on foreign-manufactured and, especially, foreign-serviced equipment presents difficulty for the A&D sector, as the amount of information that can be shared with foreign equipment service providers is limited. Although many equipment providers have U.S. based service/repair personnel, the overseas entities may need to be involved, especially regarding advanced development needs, triggering complications. The Fan-out Wafer-Level Packaging (FOWLP) equipment market provides an indicative example (see Figure 9).

### 2018 FOWLP market shares – Equipment suppliers\*

(Source: Equipment and Materials for Fan-Out Packaging 2019 report, Yole Développement, 2019)



**Figure 9: 2018 FOWLP Market Shares – Equipment Suppliers**

- 2. WORKFORCE DEVELOPMENT:** A sufficiently skilled workforce is a prerequisite for staffing the facilities needed to address the supply chain issues highlights above. Without the appropriately skilled workforce, there can be no improvement in the domestic supply chain gaps. Staffing the proposed NAPMP facilities with appropriately trained operators, technicians (process and equipment), as well as researchers, must align geographically with the location of the facilities. Universities play a critical role in establishing U.S. leadership both in research and workforce development. Emerging applications and technologies require academic research where innovations can help drive future packaging solutions that go beyond the state of the art (SOTA) today. Workforce development requires a combination of training and education where the former can be targeted towards apprenticeship while the latter on a more long-term strategy for creating future leaders. It is therefore important that

universities collectively develop a cohesive plan working closely with industry that includes professional development courses for training practicing engineers, hands-on training of technicians at two year colleges, development of package curriculum for four year and advanced degrees that includes the incorporation of emerging technologies, creating an excitement amongst K-12 students for pursuing the semiconductor area in college through the development of educational modules, and more importantly driving education through research for maintaining U.S. leadership.

**3. PROTOTYPING CAPABILITY:** Domestic packaging prototyping is strategic for long term U.S. technology leadership but is extremely limited at the leading edge of packaging. This weakness is a limitation on the domestic start-up economy. Fast system design capability together with easy access to package development and prototyping can enable a vibrant start-up ecosystem. Key focus areas include:

- **Advanced Heterogeneous Integration (HI)** including
  - High density flip chip
  - Fan-out
  - 2.5D/3D integration
- **Advanced SIP (System in Package):** High density SIP packaging is found in everything from smartphones, to wearables, to medical, to A&D applications. The overarching need is cost effective integration of hundreds of components in a small, often double-sided form-factor. This includes flexible substrates as well.
- **Co-packaged Optics:** Many photonic applications require special packaging with different types of materials that might be better suited for a dedicated electronic-photonic pilot line. Pilot lines feature manufacturing relevant processes and tooling and have enough capacity to have second-of-a-kind tooling to guarantee reproducibility, turn-around time and reliability. These lines must be accessible to small and medium manufacturers, U.S. government, and academia, and the photonics ecosystem. Manufacturing innovation institutes like AIM Photonics provide an ideal model for

development of mid Technology Readiness Level (TRL 4-6) that develop processes ready for hand off to high volume manufacturers.

- **Characterization and Reliability Labs** will be necessary to thoroughly interrogate new technologies and help assess their robustness and readiness for productization. In addition, there is need for advanced metrology tools and techniques to characterize materials and interfaces. There are a variety of facilities and capabilities required here to address the necessary standard tests and certifications. These should be co-located with the packaging technologies they service. Basic characterization capabilities provided at facilities can be complemented by advanced tools available in the NAPMP university network.

4. **LEADING EDGE DEVELOPMENT:** A governing body comprised of Industry, Academic and Government members should provide oversight to ensure tight coordination amongst the various NAPMP centers with an eye on allied research in other government facilities/programs and university work to monitor for overlaps and gaps in the technologies being pursued.

There is currently little meaningful development of leading-edge packaging technology open to the semiconductor community at large. State-of-the-art facilities are often limited to in-house usage by their owner, though some domestic industry partners are beginning to bring advanced development capabilities on-shore in an open-use model. Long term, this too is a problem but not of the same urgency as development of the supply chain and supporting workforce, and expansion of domestic prototyping capability, as detailed above.

The major packaging development hubs should be:

- **Wafer Processing Oriented:** NAPMP work on technologies that require wafer level processing like Fan-out and 2.5D/3D should be co-located together in the same facility but also co-located with the NSTC hub pursuing advanced logic scaling (1) for better cost efficiencies, and (2) due to needs for semiconductor-packaging co-design. The importance of this cannot be overstated.

- **Substrate Oriented:** NAPMP work on technologies more focused on the underlying organic substrate such as Flip Chip and SIP can be co-located but could also be geographic disparate based on resource and facility availability. This will still require co-design for advanced microelectronics with multiple technologies and increasing performance (power efficiency, frequency, noise and precision).

#### Question 4: Diverse Attributes

4. What attributes are the most important for a National Advanced Packaging Manufacturing Program to deliver? Examples include but are not limited to:
  - “Leading edge” tools
  - Characterization services
  - Collaboration across multiple universities and multiple companies
  - Development of education and workforce development infrastructure, including building a pipeline of skilled workers
  - Easy to access facility, with different processes and tools
  - Expert resident staff for custom development
  - International participation
  - Intellectual property protection for inventors
  - Open access to intellectual property
  - Post fabrication infrastructure
  - Other

**Response:**

The critical attributes of a successful NAPMP should include: (1) fair treatment of IP, (2) an easy access model, (3) service as a training facility to enable workforce development, (4) provision for research and development through prototyping and pilot line facilities to enable innovation to flourish in the U.S., and especially for small companies and start-ups, (5) Centers of Excellence focused on advancing specific technologies for which innovation is needed, (6) democratized EDA facilities for design (with AI), modeling and simulation, (7) create an avenue for the U.S. to influence important international standards as related to advanced packaging technologies. These are all critical attributes, and the numbering is not meant to confer any sense of relative importance.

**1. Fair Treatment of IP**

Some attributes to consider:

**a. Baseline NAPMP Background IP**

- NAPMP to put out a tender related to the various background IP each prototyping facility needs to conduct its R&D on a project-by-project basis.
- Industry/academia can bid and each institute can select the best package based on technical merit and cost.
- In-bound license terms would likely be non-exclusive but sub-license rights would be absolutely required (likely with royalties returning to original licensee).
- This would provide the NAPMP labs with the IP they need to initiate a new project and operate at a baseline.

**b. Foreground IP Treatment**

- Companies and / or academic institutes can join research projects for a predetermined fee, with the fee being discounted for smaller companies and start-ups.
- The fee may be paid through in-kind donations of IP, EDA tools, equipment or

materials of interest to the NAPMP if there is mutual agreement.

- Companies that join the project will have access to foreground IP with defined rights.
- Companies that did not join the project will have the right to license the IP at terms less favorable to those that were members of the project.
- The research conducted will result in foreground IP.

## **2. Access Model**

- The NAPMP should be a testbed for bleeding edge tools and materials for next generation processes / packaging structures.
- Pilot line access to the end-user community with ability to transition these technologies to full production line capabilities (and help in creating that production line).
- Provide access to early prototyping for chiplets with an Open Chiplet based I/O fabric. This allows the mix and match between technologies for new applications and workloads. Start-ups in this space can provide unique value and stimulation to this open chiplet ecosystem.
- Access to Cloud based EDA ecosystem to enable the ‘democratization’ of EDA tool access.
- A flourishing integrated ecosystem of research and development at universities, companies and federal / state laboratories to develop a highly skilled workforce and to ensure that “prototyping” capabilities remain truly state-of-the-art.

## **3. Training Facility**

Training an adequately skilled and sized workforce in the advanced packaging area will require a proactive and collaborative effort from academia and industry, sparked by government support. Work-Based Learning (WBL) programs should be offered at

NAPMP facilities. Programs that include pre-employment training, education and supportive services are an effective way to access a broad and diverse talent pool. These can be accomplished with apprenticeships, internships, cooperatives, paid work experiences, and on-the-job training programs that will lead to long term careers within the NAPMP or in industry.

#### **4. Prototyping and Pilot Lines**

Focus here on critical attributes of the pilot line for prototyping facility which needs to include processing, assembly, characterization, test and reliability enablement elements. Prototype lines easily accessible by start-up and established companies is an important consideration in helping them bridge the “valley of death” between initial concept and the generation of workable prototype devices.

Prototype facilities required for high I/O and heterogeneous integration (HI) technologies include:

- Advanced high-density laminate assembly
- Advanced FO-WLP technology and assembly
- 2.5 / 3D technology and assembly
- Advanced SIP assembly technology with a focus on automation
- Photonics co-packaging
- Ability to handle heterogeneous technologies including multiple semiconductors, sensors, photonics, interfaces and components

Note that facilities related to packaging technologies requiring wafer-level processing (e.g., FO-WLP, 2.5D, 3D) should be co-located with the NSTC.

Leading edge tools relevant to the technologies in question include:

- Processing equipment (i.e. interconnect fabric, 2.5/3D structures, etc.)



- Assembly equipment
- Process control equipment (inspection, metrology, yield analysis, etc.)
- Test equipment, both wafer probe and final test
- Characterization/Reliability equipment

The NAPMP hubs are to be positively differentiated from labs in academic setting through their 24x7 operation, second-of-a-kind (SOAK) tools, and availability of characterization, test, and reliability facilities.

Availability of skilled workers from a variety of sources are a further consideration:

- Core full-time staff
- Academics (adjunct professors, post-docs from aligned universities, ideally local)
- Corporate member assignees
- A model of permanent vs temporary staff should be developed; coupling with local universities with similar research interests can facilitate the movement and interactions of staff between the NAPMP and the university.
- The leading-edge work of the NAPMP should make it prestigious and an attractive entity to work at to progress the careers of staff supporting it.

## **5. Centers of Excellence**

Centers of Excellence (CoE) should be created to focus on advancing specific key new technologies to a maturation point at which they are transferred to prototyping facilities for integration and demonstration. CoEs should be headquartered at strategically selected locations that leverage existing local infrastructure, skills, and ecosystems. However, the work of CoEs should include universities across the U.S. to provide a source of innovations and start-ups with a five-to-ten-year horizon, and to mature education and workforce development programs that will increase and diversify the pool of talent available to

industry. To this end, the NAPMP should upgrade the infrastructure and programs at key universities to reduce the time and risk for tech transfer and to facilitate workforce investment. This will create a university network that can share facilities for both research and workforce development and also provide supplemental capabilities for the hubs and pilot lines.

## **6. Democratization of ED**

Modern cloud IT concepts should be used as a delivery platform to provide NAPMP members with access to leading edge EDA tools and AI/ML driven enhanced capabilities across design, modeling, analysis and simulation as well as scalable computation fabrics. This is particularly important for start-ups and small companies where those capabilities will be researched, enabled, and readily available to the NAPMP and NSTC participants. This is necessary to lower the cost basis for new experiments in this area.

It is also important to develop EDA tools across semiconductor and packaging. Historically these have not been delivered together. The automation of EDA tools in the Si space is much higher and needs to be extended into the chiplet-based heterogeneous integration regime. Photonic design automation, the suite of tools that support the design of chips, PICs (Photonic ICs), and packaging, it should also be included. It should be noted that these tools can be quite expensive for small manufacturers and may provide a barrier to product development in the United States. Increasingly “assembly” design kits need to be supported. Software tools will be important to connect test, measurement, and failure analysis equipment to design layouts to pinpoint issues quickly and optimize processes.

## **7. Standards**

The NAPMP should seek to set standards as related to leading edge technology it is developing in concert with established organizations like JEDEC and SEMI in this area. An open interface standard enabling chiplets from different vendors to communicate with each other on different packaging platforms would greatly facilitate an open chiplet-based ecosystem. One recent example in this space has been proposed by the Open

Compute Project (OCP) and the Open Domain Specific Architecture sub project (ODSA) (BOW – Bunch of Wires); others include AIB proposed by Intel, SuperCHIPS proposed by the University of California, Los Angeles (UCLA), and the recently announced Universal Chiplet Interconnect (UCI). Because the number of connections between chips increases as the pitch shrinks, wide parallel interfaces at slower data rates can be used in place of more complex serial interfaces, leading to the possibility of simpler hardware-based standards. This can serve as the basis for new standards to develop a roadmap for a chiplet-based interconnect fabric.

### Question 5: Factors for R&D Hubs

5. What factors are critical to enable a National Advanced Packaging Manufacturing Program to provide a successful packaging R&D hub(s)?

#### Response:

The critical factors to enable a successful NAPMP are (1) Strong Governance, (2) Clear Technical Mandate, (3) Secure and Sustainable Funding Model, (4) Accessibility, (5) Geographic Diversity, (6) Workforce Development, and (7) Security. These are all fundamental requirements, and the numberings is not meant to confer any sense of relative importance.

1. **Strong Governance:** A capable governing body comprised of experienced leaders from commercial industry, aerospace & defense, academia and government must be put in place to oversee the activities of the NAPMP, ensuring the full technical mandate is carried out without overlap between hubs and without technical gaps, and to disperse funding based on the technical agenda.
2. **Clear Technical Mandate:** The end goals of the NAPMP must be clearly stated in the form of a five to ten-year roadmap for each of the packaging platforms to be pursued and should be thoroughly informed by inputs from industry, academia, and relevant industry associations. Industry, with the most thorough, up-to-date technical, process and market knowledge should have a particularly important voice in guiding and prioritizing the work in the NSTC.

- 3. Sustainable Funding Model:** The efforts of the NAPMP must be continuous and not subjected to the ebb and flow of funding. The U.S. Government will clearly need to provide the bulk of the funding initially supplemented by industry funding over time. International organizations like IMEC, LETI, ITRI, Tyndall, and Fraunhofer Society provide models for how this may be accomplished. All of these remain dependent on government funding even decades after being launched and there should be a similar expectation for the NAPMP. However, as the NAPMP develops and matures domestic technologies for advanced packaging, it should target transition partners who can adopt those technologies and sustain them through production use.
- 4. Accessibility:** A key aspect of the “packaging hubs” is that they are accessible by small and medium enterprises, academia, the defense industrial base and U.S. Government researchers. Today much of the innovation is driven by start-ups. Having “pilot lines” which are fully capable of building complete prototype packaged systems is an important enabler for increased manufacturing and accelerated innovation in the U.S.
- 5. Geographic Diversity:** The best outcome for the NAPMP will come from leveraging the strength of our existing U.S. capabilities across the United States. The foremost facilities in the packaging areas indicated in our response to questions one, two, and three (Q1-Q3) should be sought out as the hubs for those technologies. While we specifically recommend the Albany facility for the wafer-level packaging work because of the established infrastructure and workforce and because it is co-located with the most advanced public-private semiconductor facility in the U.S., other parts of the NAPMP mission can and should be addressed in other parts of the country. The IBM facility in Bromont, Canada (just north of the Vermont boarder) should not be overlooked as a possible center of competence for advanced flip chip packaging based on their existing at scale flip chip facilities open to access by third parties (OSAT model), a long established, experienced workforce and status as a DoD Trusted manufacturing facility. Manufacturing Innovation Institutes (MII) represent an existing investment by the US Government and may be good facilities to leverage for NAPMP. Example include AIM Photonics Test Assembly and Packaging, located in Rochester, NY and also Nextflex, located in San Jose, California.

6. **Workforce Development:** It is likely that there will be critical skills gaps across the broad need for operators, technicians and researchers to adequately staff the various NAPMP hubs. These must be addressed in a timely and geographically appropriate way.
7. **Security:** NAPMP has additional unique challenges beyond entities like the NSTC, which will be critical for its success. A robust security infrastructure must be in place that accounts for the presence of many thousands of chiplets, discrete components, and other items used in complex packaging solutions. These components will be sourced from commercial companies, universities, and other entities and represent the sensitive intellectual property of the owners. The NAPMP should develop upfront solutions to acquire, store and protect these components. Additionally, access models for NAPMP assignees, internal personnel, and participating companies should be developed that optimize data sharing to maximize learning but limit access to those without an immediate need to know. A security oversight organization with a security officer might also be considered to help drive these activities.

#### Question 6: Facilities Needed

6. Identify processes, equipment, measurement capabilities, environmental conditions, and training facilities that are most crucial for facilities provided by a National Advanced Packaging Manufacturing Program.

#### Response:

Facilities provided by NAPMP should support several key initiatives with capabilities for R&D as well as prototyping for various advanced packaging technologies, including wafer level packaging, optical packaging, organic high-density substrates, advanced bond & assembly, characterization and structural analysis, including reliability testing, thermal management, electrical test, and materials characterization.

There should be dedicated facilities for R&D innovation and optimally separate prototype line facilities with an appropriate level of yield management and quality control including: (1) cleanroom floorspace, (2) equipment (sub-structure fabrication, assembly, inspection, metrology,

test, characterization, reliability), (3) specialty chemical and gases (facilities infrastructure), (4) process control, yield, and data analysis capability. As discussed in response to question four (Q4), CoE facilities should provide a complement to hub facilities.

For wafer level packaging technologies such as 2.5/3D, wafer level fan out, and wafer based optical interconnects, a silicon fab infrastructure will be required including class 100 (or better) cleanrooms with process capabilities such as lithography (resist tracks and lithography platforms) with resolution down to 0.5 micron traces / spaces (or finer) with small capture micro-via pads to enable development of pad-less via on trace interconnection density benefits.

The ability to image a wide range of resist thicknesses for various metal trace aspect ratios, enable large area stitch-less patterning, and the ability for feed-forward co-optimization for design and manufacturing can address challenges for design layout efficiency or flexibility, improved performance, and better enable design changes including die or chiplet integration changes / substitutions required for low volume / high mix or long product life and supply dynamics. Direct write maskless imaging can address die pad locational shifts during manufacturing and improve downstream process yields or cycle times for faster cycles of learning. In addition, the ability must be put in place to image large area patterning (either through reticle stitching or direct write), reactive ion etch for thru silicon via formation and other etch processing, plating processes and equipment to support copper plating (both damascene and thru-resist plating) and wafer finishing plating (Cu, Ni, SnAg, Au, and other emerging interconnect metals), chemical mechanical polish (CMP), wets (cleans, strips, and etch), wafer thinning, wafer to wafer bonding, including both permanent dielectric (fusion and hybrid) bonding and temporary adhesive bonding, wafer-to-wafer debonding, dielectric and metals deposition, organic dielectric deposition processes and equipment for temporary bonding adhesives, polyimides, epoxy mold compounds, and other organic dielectric materials as well as curing, anneal, and reflow furnaces.

In addition to these process capabilities and equipment, a full suite of metrology and inspection equipment will be required. This equipment list should include automated optical inspection, overlay and distortion measurement, ply, interferometry tools for thickness, depth, and wafer warpage measurements, and inline metrology tools. All of the equipment and capabilities listed here should be arranged in the cleanroom to enable R&D and / or prototyping of fully integrated

structures and ideally co-located with a silicon fab, as much of this equipment could be shared with Back End of Line (BEOL) fabrication lines (and in some cases co-mingled, especially for 3D processing) and will require similar facilities for peripheral equipment, chemical delivery and storage, as well as gaseous delivery systems. Colocation with a semiconductor fab will also drive significant efficiency and cost savings in terms of equipment maintenance support, training programs (particularly for infrastructure and facilities engineering), materials handling, and waste management.

The assembly facility should be housed in a class 1000 cleanroom to support scaling of interconnect pitches and hybrid bonding. Assembly equipment should include dicing equipment (mechanical, laser, and plasma), reflow and thermocompression bonding (TCB) tools, flux dispense and clean tools, pick and place tools with high alignment accuracy (same holds true for TCB tools), underfill dispense and curing equipment, dry cleaning equipment, epoxy molding compound dispense, and molding/curing for reconstituted wafer fabrication, thermal interface materials (TIM) apply and lid attach, as well as optical inspection (both die and package level), warpage measurement (for die, wafer, and substrate) and 3D imaging (x-ray) tools and equipment for rapid alignment of photonic elements.

Lab facilities (non-cleanroom) to house reliability equipment including thermal cycling and other reliability chambers as well as associated testing equipment to enable full capability for wafer level and module level reliability testing to JEDEC standards. A materials characterization lab should be facilitated to include equipment for adhesion testing, thermal properties, molecular / elemental analysis such as mass spectrometry, thermal conduction analysis, and film stress measurements. A test lab should include equipment for wafer level and module level test, including probers, test pattern generation and analysis. This lab should also be outfitted to evaluate new probe technologies to support C4 (controlled collapse chip connection) pitch scaling and micro-bump testing. There should also be a lab to support construction analysis and defect isolation. Equipment needed in this lab include wiresaw, polish, potting, x-sectional imaging, probe stations, laser ablation, cleave, and airknife tools among other equipment for x-sectional sample preparation and delayering for defect isolation. Advanced characterization tools can be available through the CoE university network. There should also be a machine shop for fabrication of various jigs, fixtures, and other peripheral parts to support these lab and assembly facilities.

**Question 6a:** How might organizations access such facilities?

**Response:**

The access model should be flexible based on different organization personas:

- Materials/Equipment suppliers
- EDA companies
- OSATs
- Semiconductor product companies (IDMs/Fabless)
- Universities
- Small companies / start-ups

Staffing should be comprised of a core full time permanent team supplemented by assignees from Member companies/Universities. It would be appropriate to have an access model similar to that described in the NSTC (in response to question seven of the NSTC response).

### **Question 7: Partnership with NSTC**

7. How closely aligned should the capabilities enabled by a National Advanced Packaging Manufacturing Program be with those provided by the NSTC?

**Response:**

There should be multiple semiconductor hubs and multiple packaging hubs. Packaging R&D and semiconductor R&D should be co-located for the case of advanced logic and HI. Hubs to support packaging for other semiconductor technologies such as memory, analog / mixed signal, sensors, flexible substrates, power electronics, and advanced SIP technologies do not necessarily need to be co-located with a semiconductor hub. There must be a governance structure that ensures tight



coordination between the NSTC and NAPMP hubs as well as ensuring tight coordination amongst the NSTC hubs and amongst the NAPMP hubs.

The NAPMP and NSTC should “act as one” since the future of microelectronics will be reliant on concurrent research and design of chips and packages. Co-design and development will enhance innovation opportunities. There are several technology areas which should be pursued by the NAPMP which will require very close alignment with the NSTC. Furthermore, there are some advanced packaging and heterogeneous integration technologies which require the same infrastructure and process capability as the NSTC, so it would be highly desirable to co-locate some areas of the NAPMP and the NSTC. In fact, there are some technologies where it would be extremely difficult if not impossible to enable without co-location of the NSTC and NAPMP. The technologies that should be considered for co-location fall into the category of the wafer level packaging and include 2.5D and 3D integration, advanced wafer finishing, interconnect scaling (including advanced micro bump and hybrid bonding) and high density wafer level fanout. These technologies are currently being advanced by leading foundry players and are leveraging this co-location synergy for this reason. If the U.S. does not promote the “blending” of Si and wafer level packaging technologies through pre-competitive infrastructure and other incentives, it will lose a competitive edge in this emerging technology field which will be crucial for next generation computational hardware technologies. For example, 2.5D and 3D packaging requires the integration of thru silicon vias (TSVs) in the device wafer during the fabrication of the BEOL levels which must be done as part of the process flow for fabricating a silicon chip. The wafer must then be thinned from the wafer backside to expose the TSVs then one or more BEOL levels must be fabricated on the backside of the wafer to form contacts to enable stacking of wafers (or individual die) with electrical interconnects between the layers of silicon in the 2.5/3D stack. This full process sequence must be enabled in a silicon fab, which is why the facilities and teams for enabling these types of wafer level packaging technologies should be one and the same as the facilities and teams for enabling silicon chip fabrication.

Capabilities for photonics and co-packaged optical interconnects and assembly should also be closely aligned with the NSTC, as much of the process capability for these technologies relies on similar toolsets as those required for silicon and advanced packaging, including capabilities for optical waveguides and high precision assembly. As optical interconnects are becoming more

viable for on- module and short reach applications, it will be critical to have closely aligned or co-located facilities to enable the seamless integration of these technologies for co-packaged optical – electrical applications.

It should also be noted that design infrastructure (EDA tools) is evolving to encompass co- design of silicon chips and advanced packaging, so it will be essential to have design infrastructure that supports both silicon and packaging design seamlessly. Electrical test and failure analysis facilities are also essentially the same for both silicon and wafer level packaging, so it will be crucial for the capabilities to span both the NSTC and the NAPMP.

Facilities requirements for fabricating organic substrate-based packages for 1st and 2nd level packaging applications are not as rigorous as silicon fabrication/wafer-style assembly requirements, so this capability does not require as close alignment with the capabilities for the NSTC. However, organic package assembly development should be closely aligned to ensure that advances in the interconnect technologies across these technology elements are well coordinated to enable efficient development and deployment of a complete assembled module technology solution. The same argument holds true for other packaging form factors such as flex, wearables, sensors, etc.

### **Question 8: Partnership with National Network for Semiconductor R&D**

**8.** How should the National Advanced Packaging Manufacturing Program connect to National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA? What considerations should be given to ensure strong integration between the two efforts? Should there be overlap in the technology readiness levels served by each program? How should the National Advanced Packaging Manufacturing Program connect to National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA?

#### **Response:**

It is critical that the research agendas and technical capabilities of the commercially focused NSTC

and NAPMP and the DoD funded National Network for Microelectronics Research and Development (NNMRD) be coordinated. Both DoD and commercial companies are united in their need to identify viable emerging technologies, including those containing novel materials & devices, circuits & architecture, of high impact to the semiconductor supply chain, start-up, & manufacturing eco-system. A university network of the NSTC and NAPMP would most likely have synergy with the research agenda of the NNMRD. Thus, close coordination of infrastructure investments within the university community will be needed to avoid duplication and maximize broad leverage across programs. Additionally, security and protection of domestic IP are concerns shared by both commercial and defense programs. However, the NSTC and NAPMP, should be focused on commercial industrial leadership, and should not be affected by defense-specific security, ITAR restrictions, or niche defense needs. Mission areas that DoD values highly but are not as applicable to industry may also be identified for NNMRD focus. Dual use and viable technologies and designs matured through the NNMRD can be developed further and tested out through prototyping within the NSTC and NAPMP and readied for transfer to manufacturing facilities. It is essential that if there are trusted/assured requirements for DoD technologies, that they be comprehended early on in the planning phase for the NSTC and NAPMP to minimize impact on physical layouts, IT security, and personnel issues.

There must be tight cross-agency coordination focused on the strategic implications of the future of semiconductors. An important distinction between the DoD work and that of the NSTC and NAPMP is that DoD will also likely include work at the classified level, while the NSTC and NAPMP will have a commercial focus. To the extent possible, it would be useful if both entities could use the same tools, techniques, flows, etc. to avoid fundamental obstacles from crossing over from one to the other.

Inter-agency coordination is needed, for example, as DARPA alone has multiple semiconductor related research projects in addition to its ongoing portfolio of Microsystems Technology Office (MTO) projects. These include programs such as:

DARPA Electronics Resurgence Initiative (ERI): Government-industry partnership investing to support a domestic semiconductor manufacturing sector that implements specialized, secure circuits that can be trusted through the supply chain. This comprises 3D heterogeneous integration,

new materials and devices, specialized functions, and design and security. It includes participation from industry, defense, and academia; and

DARPA Joint University Microelectronics Program (JUMP): Partnership between DARPA and the Semiconductor Research Corporation working to increase the performance, efficiency, and capabilities of electronic applications.

Additionally, beyond the NSTC/NAPMP/NNMRD coordination, there are multiple U.S. government initiatives in NSF, DoE, DoD and DoC to promote semiconductor innovation and production. It is very important that these programs be coordinated and integrated into a cohesive national strategy. In particular, it is imperative that through the aggregate of these programs, suitable investments in the university microelectronics infrastructure are made that enable universities to carry out their critical functions. The different priorities, strategies, incentives, and culture of the multiple agencies involved makes this type of coordination complex but critical for the U.S. to optimize its investment strategy.

To bridge the so-called “valley of death”, a funding and resources gap between “lab to fab”<sup>9</sup>, a tight connection between the DoD NNMRD and the university network of the NSTC and NAPMP is needed. Thus, an overlap of Technology Readiness Levels (TRL) may be required, especially between levels three and four where a technology has been validated in a lab. Technologies matured through the NNMRD can be transitioned into the NSTC and NAPMP for prototyping, and eventually an overlap in TRL six and seven is also expected for transfer to manufacturing. Therefore, the unique capabilities of NSTC and NAPMP enable advanced prototyping and fills the gap, or missing capability, in today’s American semiconductor ecosystem, and would serve both commercial and government needs. For a seamless transition between the DoC and DoD networks, an agreed-to set of TRL definitions would also be required as in practice, agencies define TRL’s slightly differently. In addition, the trusted/assured requirements for DoD technologies will need to be comprehended to enable secure prototyping in the NSTC and NAPMP. Finally, it should also be pointed out that while overlap of TRL may be needed, this does not necessarily imply technical overlap, as the NSTC and NNMRD may have different technology focuses.

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<sup>9</sup> American Innovation, American Growth: A Vision for the National Semiconductor Technology Center,” MITRE ENGENUITY, 2021.

### Question 9: Education and Workforce

9. Describe anticipated needs in education and workforce development, including retraining and upskilling, in the semiconductor packaging area.

**Response:**

Due to the absence of a substantive advanced electronic packaging ecosystem in the U.S., the needs in education and workforce development needs are extreme. The current needs are already high as demonstrated by the long time that it takes to fill open job positions, and this trend is expected to become worse as packaging technologies become even more complex and the competition for talent increases with the anticipated staffing needs of the new semiconductor fabs announced in the U.S.

Education in semiconductor technology typically focuses on fundamentals of device and chip design. However, the semiconductor packaging area requires unique skillsets (most closely related to mechanical engineering and materials science disciplines) that can only be best learned through on-the-job training along with the advanced electronic and electronic/photonic packaging curriculum, and through increased visibility of packaging fundamentals in community college and university curricula. Examples of these jobs are diagnostics and failure analysis engineers, engineers and researchers able to carry out electrical, thermal, mechanical, process, reliability and optical modeling, and materials scientists and engineers needed for the development of new packaging materials, to name a few. This area requires a workforce with unique interdisciplinary skills, making the job of staffing even more challenging. Different parts of the workforce will require various levels of education ranging from high-school graduates through university graduates with advanced degrees.

Current programs are inadequate to support a sustained and widescale U.S. initiative to develop a domestic advanced electronic packaging industry base. The workforce needs both in the incumbent worker space (for reskilling and upskilling) and in the incipient worker space (i.e. students currently or soon-to-be enrolled in relevant two-year, four-year and graduate degree programs) are substantial. A packaging curriculum does not broadly exist in academic institutions today. The

curriculum needs to be developed with a series of course offerings, which then are offered to students who will take internships or research projects at the NAPMP.

**Question 9a:** How adequate is it currently, and what are future expectations of need?

**Response:**

In the semiconductor packaging area, current efforts in education and workforce development are inadequate to support a sustained and widescale U.S. initiative to develop a domestic advanced electronic packaging industry base. The expectation is that the skillsets needed will become even more scarce in the future unless proactive action is taken. The projected scarcity comes from an aging demographic, increased competition for the small talent pool with skills in packaging design, heat transfer, thermal and stress modeling, and an increasing complexity in packaging technology, further exacerbated by a lack of student interest and awareness in this field.

**Question 9b:** How should the workforce training pipeline be developed?

**Response:**

Work-Based Learning (WBL) programs that include pre-employment training, education, and supportive services are an effective way to access a broad range of talent pools. These include apprenticeships, internships, co-operatives, paid work experiences, and on-the-job training programs.

Pipeline development is crucial and should be carried out in parallel efforts: (1) Leverage current college/university programs to coordinate student access to full-flow packaging lines within NSTC and NAPMP (e.g. AIM Photonics Test, Assembly, and Packaging (TAP) prototyping center in Rochester, New York). In parallel, standalone reskilling/upskilling programs should be rapidly deployed at the same type of full-flow facility. (2) It will be necessary to develop educational modules in advanced electronic and electronic/photonics packaging that can be quickly deployed in adjacent academic degree programs (i.e. semiconductor technology related programs) to impact

students that are preparing to transition to the U.S. semiconductor workforce. (3) For longer-term impact, federal assistance should promote targeted development of new academic courses of study across the U.S. higher-education community in close collaboration with semiconductor packaging employers to expand the workforce pipeline at a rate concomitant with employer need. Investing heavily in training/education programs without a corresponding initiative in matching graduates to existing jobs is a noneffective strategy. Also, there must be incentives to direct faculty renewal and hiring towards the semiconductor sector.

Community college programs involving courses and internships can be developed in collaborations among universities, industry, and NAPMP facilities. The pressing need for new engineers can be addressed by attracting students to careers in advanced packaging through exposure to the fundamentals of packaging technology in new curricula and university-based hands-on experiences. These should be coupled with internship opportunities in industry and NAPMP facilities. Expanded capabilities for industry-relevant university-based research will also provide the future industry leaders that will drive innovations needed to reassert leadership in packaging technology and manufacturing. This requires incentives that will direct faculty renewal and hiring towards the semiconductor sector.

All participants in NAPMP activities must engage in K-12 Science, Technology, Engineering, and Mathematics (STEM) outreach activities to communicate excitement about career opportunities in the semiconductor industry and the impact such careers can have in addressing societal needs. Awareness of the industry and what it enables is a major hurdle for inspiring students to pursue education relevant to the semiconductor industry. Applications-based lessons developed in partnership with educators would help K-12 students understand the importance of semiconductors in their lives. Providing teachers with opportunities to become comfortable enough with a subject to want to include it in their already full curriculum is key to students learning about it. Professional development opportunities, workshops, and Research Experiences for Teachers programs are all ways to support teachers in including relevant topics into young students' education. The semiconductor industry can support this effort through stipends, funds for classroom supplies, providing tours and guest speakers, and by participating in research experience programs.

## SEMICONDUCTOR WORKFORCE

### Question 1: Occupational Shortages

1. What are the greatest occupational or skills shortages facing employers in the semiconductor sector?

#### Response:

The skills shortages in the semiconductor sector span a broad range of areas including early-stage research and prototyping, high volume manufacturing fabrication, semiconductor supplies, and semiconductor design and verification:

**Fabricator:** Within the fabricator (“fab”) skills shortages range from the facility engineering team (high school, two-year degree, BS, MS) required to operate a clean room within a safe and productive environment, to process engineers (two-year degree, BS, MS, PhD) that operate the tools, to research engineers (MS, PhD) who innovate new types of chips and ways of making them, and software engineers (two-year degrees, BS, MS, PhD) that use AI-based learning approaches to improve process yield, tool status, and fab logistics.

**Suppliers:** Suppliers to the semiconductor manufacturing sector face similar challenges. Across the value chain there is a lack of skilled workers who are knowledgeable and capable of working in a controlled environment such as a clean room. In addition, there is a shortage of process and research engineers that combine skills in chemistry, chemical engineering, physics, and materials science with skills in data analytics that are needed to make data-driven decisions.

**Design:** Another major skills shortage is in semiconductor design, verification, and post-silicon validation, in creation of innovative design tools, and advanced packaging design. The increasing complexity of computer architectures, multi-chiplet heterogeneous systems, and electronic design automation (EDA) technology, drives the need for skilled design and verification engineers to ensure first-pass silicon success. This requires skills in co-design with architecture and applications. The workforce for the EDA industry also faces challenges from



other industries competing for similar software skills, as well as a dearth of new talent from academic institutions.

**Packaging:** There is also a substantial shortage of talent with advanced packaging skills, both in the design and fabrication spaces. Increasing complex multi-chiplet heterogeneous systems assembled with advanced packaging needs significant co-design with emerging applications. This shortage limits domestic industry from developing this critical link in the semiconductor ecosystem and overall supply chain.

**Construction:** As the number of semiconductor factories in the U.S. expands, there is a substantial shortage in construction and trades workers that are essential to new factory construction, equipment installation, and facility operation.

**Question 1a:** What are the consequences of those shortages with respect to the domestic operation of employers in the sector?

**Response:**

The lack of highly skilled semiconductor technicians and engineers will derail efforts by semiconductor companies in the U.S. to stay at the forefront of advanced technology and remain competitive in a global market, especially with the growing complexity of design, fabrication, and packaging of chips that are required to serve new high-growth markets like AI, Cloud, Quantum, and 6G communications. These are markets that the U.S. helped to create through long-term investments in applications of semiconductor technology but the semiconductor sector skills shortages threaten the U.S.'s ability to reap the economic benefits of these emerging technologies.

These skill shortages will impact not only innovation, but also the timely construction of factories, as well as the overall semiconductor production that impacts all downstream markets (e.g., automotive markets). All these directly translate to increased costs and further limit the U.S. share of global semiconductor production. For example, shortages in fab-facility engineers and equipment technicians will impact overall chip production; shortages of development engineers will slow the adoption of more advanced semiconductor processing flows; shortages in advanced

packaging technicians and engineers will limit the ability of the U.S. to establish a leadership position; and shortages of constructions and trades skills slow down the establishment of new factories that are needed to re-establish the domestic semiconductor supply chain.

These skill shortages do not only impact employers, who are at the consumption end of the talent pipeline. The lack of semiconductor sector technician and engineering talent, for example, exists at the ‘entrance’ and ‘along the length’ of the workforce education and training pipeline. Without sufficient talent choosing these paths, it threatens the existence of even current two-year, B.S., M.S., and Ph.D. programs that support the semiconductor workforce, leading to a vicious circle of depressed education and training opportunities for semiconductor sector careers.

To cope with these skills shortages, some companies have moved these roles offshore, including to countries such as Singapore, China, and India, which have been, for example, strategically and quickly increasing the numbers of analog, mixed-signal, and digital designers.

Developing a skilled labor force at the scale and speed necessary for the U.S. to regain leadership in semiconductor manufacturing requires a significant ramp-up in university research funding and facilities upgrades balanced with new education program funding that can provide institutions across the nation to deliver curriculum and hands-on training in partnership with the semiconductor industry.

**Question 1b:** Considering all aspects of building, equipping, and running semiconductor manufacturing and R&D facilities, what actions have been taken to address these shortages, how effective have they been, and what gaps remain?

**Response:**

For semiconductor production, development, and research, an effective strategy to mitigate workforce shortages has been to directly engage industry with higher-education providers and training institutions. Several examples indicate that when this is done in a particular region or in a particular segment of the industry, it serves to improve the local education and training pipeline and expand the pool of qualified candidates and workers. In particular, such partnership between

industry and academic institutions serve to better match academic degree programs with industry needs and increase job readiness of the workforce through hands-on experiential education and training.

Examples of such partnerships and their impact are described below:

1. The [New Silicon Initiative](#) (NSI) prepares students for careers in hardware technology and silicon chip design via curriculum development, tape-out cost, and the creation of post-silicon validation labs at participating institutions. The NSI also provides an internship pathway for undergraduate and graduate participants. This establishes an industry-ready talent pipeline at different degree levels. First rolled out across seven universities (Alabama A&M, Berkeley, CMU, Howard, Prairie View, Morgan State, Stanford), this is an effective and scalable, industry/educational model. The NSI also provides an internship pathway for undergraduate and graduate participants.
2. Industry-academia partnerships enable the use of commercial grade tools instead of academic versions, whether proprietary or open source, and accelerates students' job readiness. Utilizing online tools improves accessibility of training. Another example is a collaboration between Google and Efabless that has supported over 200 tape-outs at SkyWater Technology. Another example is the use of Efabless "OpenLane" ASIC flow by Bangalore-based VLSI System Design to train over 2,500 students over the past three years, with over 10% of the students residing in the U.S. In another example, Cadence Design Systems provides commercial-grade computer-aided-design tools, low-cost measurement devices, and a lab-in-a-kit in partnership with North Carolina State University and local community colleges. Participants in this program learn through online digital media, then design, build, and test foundational building blocks of electronic sensing and communications systems.
3. University-based, cutting-edge chip facilities that have been created in partnership with industry have also offered substantial experiential learning opportunities and have helped to close key gaps in student skill attainment. NY CREATES' 300mm pilot facilities in Albany, New York routinely hosts two-year, four-year and graduate level interns to provide hands-on experiential learning to promote transition directly in the semiconductor industry.

These opportunities need to be expanded through a hub-and-spoke model to broaden access to a larger network of educational institutions across the country. Simultaneously, such a distributed network of a few 200mm facilities at universities nationwide would allow for both cost-effective research advancements in novel semiconductor devices/systems, analog electronics, and novel materials beyond silicon.

4. In terms of better connecting existing technician and engineer degree programs (two-year, BS) with industry, a successful example involved a group of regional chip sector companies in upstate New York providing educators with direct access to their specific skill/competency needs so that a range of existing degree programs could be reasonably aligned to improve student preparation. This ‘alignment’ of industry needs with educational programming substantially improved the ability to tap into the local talent pool. This activity has resulted in the development of a scalable industry/educational alignment platform – the National Institute for Innovation and Technology (NIIT) National Talent Hub. Sponsored by the National Science Foundation (NSF) in partnership with the NIIT, SEMI, SUNY, and various industry partners (Applied Materials, Tokyo Electron, LAM Research, KLA-Tencor, GlobalFoundries, ON Semi, Wolfspeed, Edwards Vacuum, among others) the National Talent Hub is an online portal where industry can provide competency needs for their workforce and education providers can provide competency profiles of their existing programs. It enables educators to efficiently align their programs to industry needs and provides employers with a detailed profile of competencies of graduating students. First rolled out in the New York and North Carolina regions, the National Talent Hub this is an example of a new, scalable model to effectively connect students with chip industry employers.
5. In the area of fab construction there have been past partnerships between government, industry organizations and fab construction companies to establish training centers. For example, a regional partnership between New York State and M&W group (now Exyte), a global construction and design firm for ‘fab’ construction, established a semiconductor construction-trades training program at the Watervliet Arsenal in Troy, New York to support regional fab construction. Although no longer in operation, partnerships such as

this should be reexamined and reimagined through federal government support to provide key skills to our construction and trades workforce to support the semiconductor industry.

6. Relevant to Advanced Packaging Technologies, AIM Photonics, a U.S. Manufacturing Innovation Institute, has recently partnered with New York State and industry to establish a Test, Assembly, and Packaging (TAP) prototyping center in Rochester, New York, to support advanced packaging R&D, prototyping, and workforce development. Incorporating a full electronics/photonics packaging line, the TAP facility provides hands-on experience for student and incumbent worker training. In doing so, the center fulfills an essential need for hand-on training for students to develop the necessary skills to enter industry. Considering the critical importance of advanced electronics packaging to U.S. competitiveness, it is essential to leverage these types of partnerships to expand advanced packaging training access.

However, several gaps remain, and they are summarized below:

- A. Despite regional successes of some of the programs mentioned, their aggregate impact to date has not been sufficient to address the workforce shortages across the U.S. and will clearly need to grow at a national scale with a more coordinated cross-agency and cross-industry effort (including government support) to address this crisis. Successful national scaling of semiconductor workforce programs must engage educational organizations of sufficient size and breadth to ‘move the needle’ with respect to student recruitment, education, and effective transition to employment across the breadth of the semiconductor workforce. Large higher educational systems (e.g., the State University of New York, University of Texas, University of California/California State University, etc.) must be leveraged for their large access to a broad and diverse student body and the necessary range of academic programs (A.A.S., A.S., B.S., M.S., Ph.D.). Other national networks of colleges and universities must also be leveraged. The Historically Black Colleges and Universities (HBCU) network and the scores of minority-serving academic institutions (MSIs) across the U.S. must be engaged. Many of these institutions have, historically, not been strongly engaged with the U.S. semiconductor industry, and represent a rich, untapped resource for the semiconductor workforce.

- B.** In addition, there are substantial gaps in student and incumbent worker engagement programs to increase awareness of semiconductor manufacturing careers and encourage employment in the industry. Intentional efforts to foster diversity, equity, and inclusion are needed to provide access to students who traditionally would not pursue careers in semiconductor technology. This is not only critical for the career opportunities that currently exist, but even more important for the next generation of semiconductor industry workforce.
- C.** For hardware training, students should be exposed to high quality toolsets within the university shared research/educational facilities, requiring a nation-wide upgrade of the university semiconductor research infrastructure, and access to learn on industry grade toolsets that could become available in collaboration with industry partners.
- D.** The ability of students to complete an internship or a cooperative assignment within industry or at an industry-aligned semiconductor development facility has been successful towards expanding transitions of students in the BS/MS/PhD pipeline to semiconductor programs. However, gaps remain in terms of the number of internships that can be supported by a given semiconductor company. Similarly, apprenticeship and work-based learning (WBL) programs are key recruitment initiatives that proactively address skills gaps that don't require a college or advanced degree and accelerate the worker's ability to contribute at a higher level of productivity and expand the available pool for hiring. Incentives and support for the hiring and training of interns, co-ops, and apprentices, would provide far more of such opportunities.

## **Question 2: Strategies for Mitigation**

- 2.** What strategies have been most effective in addressing the shortages?

### **Response:**

Providing access to curriculum and hands-on training to a wide range of institutions including two-year community colleges, vocational training institutions, and technical high schools, helps to

build the foundation for younger students and enable rapid retraining for workers transitioning from other industries. Examples include industry/university-based consortia such as NY CREATES' world-class 300mm pilot facilities in Albany, New York, as well as other 200mm and 150mm shared open facilities that are located at research universities across the country. Similarly, the AIM Photonics Testing, Assembly, and Packaging (TAP) facility in Rochester, New York, is an excellent example of a new federal/state partnership that opens cutting edge electronics packaging facilities for workforce training. A distributed nation-wide network of such facilities of different sizes tailored to local needs will provide critical access for research advancements and training the workforce.

Work-Based Learning (WBL) programs that include pre-employment training, education, and supportive services have also been effectively used to access a broad range of talent pools. These include apprenticeships, internships, co-operatives, paid work experiences, and on-the-job training programs. As an example, with the support of the industry, SEMI is developing pre-apprenticeship and apprenticeship programs as well as curriculum at high schools and community colleges that have the potential to scale nationwide but need significant investments. SEMI is also working with industry on developing stackable credentials for incoming workers to further legitimize the programs with member companies, increase worker mobility, and propel workers into filling current open opportunities.

**Question 2a:** Which states or countries have created the most effective strategies for different types of workforces needs to build, equip, and run semiconductor manufacturing and R&D facilities?

**Response:**

The most effective strategies are those that coordinate across academic institutions, training organizations and cross-industry, most often with underlying government support. Several examples are detailed below.

## U.S. Programs

1. An example that illuminates best practices for coordination between governments, educators, and industry is seen in from the Manufacturing Institute<sup>10</sup> (MI) which is focused on growing and supporting the nation's skilled workforce for the advancement of modern manufacturing. The MI's diverse initiatives support all American workers, including emerging workers, women, veterans, and students, through skilled training programs, community building and career growth.
2. The Department of Defense (DoD) recognized the need to interest undergraduates in pursuing a microelectronics career in the DoD, a result of the confluence of its aging workforce and its growing requirements to design, build, and maintain high performance, cutting-edge electronics in demanding environments. The DoD IBAS (Industrial Base Analysis and Sustainment) program is focusing on developing and implementing a wide range of novel solutions for technician training at the community college and undergraduate level. The DoD SCALE program (Scalable Asymmetric Life Cycle Engagement) is based on a multifaceted model to attract, retain, motivate, and train undergraduates about microelectronics. Starting in the first undergraduate year of study, the program helps students make meaningful connections to the DoD through mentoring and internships and provides hands-on and relevant experiences in high priority topics in defense microelectronics. The first five technical tracks (known as "verticals") are radiation hardened electronics, heterogeneous integration and advanced packaging, system on chip, embedded system security, and supply chains. With sixteen partnering universities, over twenty DoD facilities, and over twenty companies in the defense industrial base (DIB), there has been joint curriculum development and delivery, development of recruitment and retention strategies, and rigorous assessment of what is working and what is not. Of specific note is the DoD working with the universities to define and teach the knowledge, skills, and abilities (KSAs) needed across the board for all topics as well as for the technical verticals for specific jobs within the DoD and in the DIB.

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<sup>10</sup> <https://www.themanufacturinginstitute.org/>



## State Programs

1. A specific example for the semiconductor industry is the National Institute for Innovation and Technology (NIIT) National Talent Hub, an online portal where industry can provide competency needs for their workforce and education providers can provide competency profiles of their existing programs. This enables educators to efficiently align their programs to industry needs and provides employers with a detailed profile of competencies of graduating students. First rolled out in the New York and North Carolina, regions, this is an example of a new, scalable model to effectively connect students with chip industry employers.
2. An example of a statewide initiative is the Massachusetts Manufacturing Innovation Initiative (M2I2), which has established a very innovative network, the Lab for Education and Application Prototypes (LEAPs), which serves to educate and train not only its own student population, but also students from nearby community colleges. The LEAPs are comprised of academic centers teamed with local industry with a strong mission:
  - a. Education: Develop the next generation workforce through sponsored research programs, summer internships, summer academy, bootcamps and workshops, online manufacturing courses, and Virtual Reality (VR) for training in advanced manufacturing.
  - b. Application Prototype Development: Create prototypes in partnership with start-ups and subject matter experts by innovating in components/tools/processes and applications research.

In the past two years since the inception of the LEAP network, over 50 students have participated in training, which is an impressive number for such hands-on programs.

3. Several large, coordinated, educational systems in the U.S. have demonstrated success in supporting the semiconductor workforce. For example, several educational systems including the State University of New York (SUNY), University of California, Purdue, Georgia Tech, RPI, MIT, Cornell, and many others have proven track records of training a skilled workforce to meet a broad range of semiconductor jobs. This includes training for engineers and R&D level professionals in leading-edge semiconductor designs and technologies through the

combination of research and education. It also includes cooperative education programs involving work periods in industry during the BS degree. Community college and technical high schools that train the skilled technical workforce necessary for chip manufacturing and advanced packaging are a key component in the talent pipeline and have also demonstrated success, but face challenges in scaling this success due to lack of resources.

## International Programs

1. In Europe, there are several examples of on-the-job training and talent pipeline development. The Marie Skłodowska-Curie Actions<sup>11</sup> includes several programs such as Doctoral Networks that bring together multiple diverse stakeholders, Postdoctoral Fellowships that are tailored to increase mobility of talent and diversity of expertise, and Staff Exchanges that develop sustainable collaboration between experts in different sectors. The National Centers of Competence in Research<sup>12</sup> program by the Swiss National Science Foundation has created 42 centers based at higher education institutions to promote long-term research networks with a focus on the education and promotion of women. Programs such as these show us ways of establishing collaborative networks with government support to accelerate the pipeline from education to jobs.
2. In Asia, several countries have focused programs to accelerate and sustain a semiconductor workforce. In Taiwan, National Tsing Hua University is setting up a new College of Semiconductor Research. In China, Peking University has set up the School of Integrated Circuits to train chip engineers and technicians. In many instances, these universities have formed partnerships with industry to align skills and training with specific demand. Institutions such as TSRI (Taiwan Semiconductor Research Institute) bring together academic and industry partners to conduct leading leading-edge research and to accelerate the path from research outcomes to technology commercialization.
3. Canada has created and funded CMC Microsystems<sup>13</sup>, which has ensured that Canadian universities can all take advantage of commercial-grade tools, curriculum, support and

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<sup>11</sup> <https://ec.europa.eu/research/mariecurieactions/>

<sup>12</sup> <https://www.snf.ch/en/EcRzGgwFJMZjfnNe/page/national-centres-of-competence-in-research-nccrs>

<sup>13</sup> <https://CMC.ca/>

computer resources. This has reduced the Computer Computer-Aided Design (CAD) overhead for both the faculty and students to ensure that they can focus on teaching critical concepts. This has also been shown to be critically helpful for research teams and across-university collaborations. Similar challenges have been highlighted in U.S. schools, and such programs can help to alleviate these challenges.

It is imperative for the U.S. to accelerate partnerships of these types to not only promote specific skills and competencies in various education and training programs, but to stimulate participation of U.S. students in semiconductor career pathways.

**Question 2b:** What industry or other credentials do employers use, or could use, to train and hire workers to fill needed positions?

**Response:**

Currently, there are no widely recognized semiconductor workforce standards or credentials across the semiconductor industry, and this is a critical gap. Only recently (2020), has the DOL-ETA (Department of Labor Employment and Training Administration) added an advanced manufacturing competency model including semiconductor sector competencies to its competency model clearing house site for the technician workforce<sup>14</sup>. To effectively develop a semiconductor workforce requires expanding industry-led national standards and goals for semiconductor workforce education, especially in areas of design, fabrication and advanced packaging that involve the newest and most powerful technologies. While the new semiconductor DOL-ETA competency model standards can provide two-year institutions with a baseline for educational requirements for curriculum alignment and for a worker-based learning apprenticeship program, parallel efforts are needed to expand goals for semiconductor workforce education in the areas of semiconductor design, engineering, and advanced packaging curricula. A credentialing infrastructure, similar to the trades (electricians, plumbers etc.) and an appropriate engineering licensing examination structure (such as Professional Engineer for civil engineers) needs to be implemented, along with a university accreditation in semiconductor technology. A partnership of

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<sup>14</sup> <https://www.careeronestop.org/CompetencyModel/Competency-Models/advanced-manufacturing.aspx>

community colleges, R1 (doctoral) universities and industry can be established to align on the curriculum. These credentialing standards are essential to increase worker mobility and enable the industry to tap into a nation-wide workforce.

In addition to the DOL-ETA competency model in the semiconductor sector for the technician workforce, the semiconductor industry could learn from the broader model set by the National Institute for Innovation and Technology (NIISTNIST) National Initiative for Cybersecurity Education<sup>15</sup>, which has developed a framework in partnership with academia and the private sector that establishes national standards for a cybersecurity workforce. While specific standards for educating a semiconductor workforce do not yet exist, the American Society for Testing and Materials (ASTM) International does recognize educational standards for undergraduates in nanotechnology health and safety, pattern generation, characterization, and infrastructure<sup>16</sup>. These cover several relevant skills, particularly at the technician and community college levels. In Europe, the European Skills Agenda<sup>17</sup> recognizes the importance of a systematic approach to classifying jobs and skills through partnerships of public and private organizations. This mirrors the nascent National Institute for Innovation and Technology (NIIT) National Talent Hub developed by NIIT, SEMI, SUNY and the National Science Foundation (NSF).

In another example of industry leadership on credentialing in semiconductor design, Cadence has opened commercial online courses to students that provide digital badges and offer a credential that employers recognize, that could be replicated more broadly. Since 2016, over 500 computer engineering master's students at UC San Diego have taken between one and three of the Cadence online training courses as part of an Application Specific Integrated Circuit (ASIC) implementation class. This is a scalable and easily deployable approach that can provide a critical foundation for engaging a variety of STEM programs across the U.S. that enroll underrepresented minorities so that they have more effective access to the semiconductor workforce. Such programs also allow workers with the relevant skills from other adjacent industries to transition into the semiconductor industry.

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<sup>15</sup> <https://www.nist.gov/itl/applied-cybersecurity/nice>

<sup>16</sup> <https://www.astm.org/catalogsearch/result/?q=nanotechnology>

<sup>17</sup> <https://ec.europa.eu/social/main.jsp?catId=1223https://ec.europa.eu/social/main.jsp?catId=1223&langId=en>

An important additional factor to consider, is the potential role of accreditation in developing highly effective education and training programs in microelectronics. The Accreditation Board for Engineering and Technology (ABET) is the global leader in accrediting college and university programs in applied and natural science, computing, engineering, and engineering technology at the associate, bachelor's, and master's degree levels. While the current scope of ABET accreditation is on those four standard degrees associated with widely recognized "disciplines", ABET could play an important role in developing education standards for certificates and minors in areas of high national need, such as microelectronics and sustainability. With its reputation for quality, best practices, and impact, ABET is well suited to tackle this in close collaboration with the microelectronics industry and universities.

**Question 2c:** To what extent do employers in the semiconductor sector partner with government institutions such as local workforce boards, economic development organizations, or Manufacturing Extension Partnership centers, or international partners to establish training and/or skill certification programs?

**Response:**

Overall, partnerships with semiconductor employers, industry associations and government institutions are limited. However, in addition to the U.S. partnerships discussed previously, one highly successful initiative has been the establishment of P-TECHs<sup>18</sup>. Created through partnerships that combined the expertise of public and private institutions with government support, P-TECHs comprise a merged high school/two-year college curriculum that students complete concurrently to obtain a high school diploma and an associate degree.

P-TECH was designed with two goals:

- 1) Address the global "skills gap" and strengthen regional economies by building a workforce with the skills required for new-collar jobs and

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<sup>18</sup> <https://www.ptech.org>

- 2) Provide underserved youth with an innovative education opportunity and direct pathways to college and career readiness.

P-TECH Industry Partners enable students to participate in a range of workplace experiences, like internships and apprenticeships, that support student completion of their two-year postsecondary degree and prepare them to either continue their education or begin entry-level careers. Last year, IBM offered 1,000 new paid internships for P-TECH students and graduates.

IBM's [New Collar](#) training programs were developed to allow students to follow non-traditional paths into productive industry employment. These have been designed such that other companies, organizations, and governments can easily adopt and scale, even when IBM isn't directly involved. There are more than 600 industry partners in P-TECH schools that have joined with more than 20 top U.S. companies to expand apprenticeships across the U.S. IBM teamed with the Consumer Technology Association (CTA) to create the CTA Apprenticeship Coalition and provides frameworks, playbooks, and guidance for others to create or expand their own apprenticeship programs.

Additionally, the SEMI Foundation has created a partnership with government institutions, workforce boards, economic development organizations, and community partners and has launched the SEMI Career and Apprenticeship Network (SCAN) at the request of the Department of Commerce (DoC). The objectives of SCAN are to build a national apprenticeship and network model with the overall goal to transform local, regional, and national economies.

**Question 2d:** To what extent do employers in the semiconductor sector partner with other employers to create joint training programs?

**Response:**

In terms of workforce training, the U.S. semiconductor industry has primarily limited its joint efforts to pre-competitive Research and Development (R&D) wherein workforce development efforts are largely comprised of industrial funding of graduate students in various STEM fields

through organizations such as the Semiconductor Research Corporation (SRC) or former industry consortia such as SEMATECH.

SRC<sup>19</sup> is an example of long-term collaboration across multiple employers in the semiconductor industry with government and academic institutions to develop an expert semiconductor industry workforce. Industry and academia partner to fund basic research in areas critical to the semiconductor industry. In addition to the important technologic advances, this program has helped train the next generation of semiconductor innovators. With additional government support, these types of partnerships can be expanded and multiplied across the nation, to address the workforce gaps, with a focus on creating a diverse pool of candidates by including minority serving institutions.

Key to the success of industry-led workforce-training programs is the close engagement of university partners in developing both research and educational objectives. Universities are best suited to provide for the student's educational needs that would match the expressed job-training needs of the industry partners. The diminishment of the training of the semiconductor professionals in U.S. universities is directly related to the diminishment in research/education funding provided by industry for preparing the next generation of technical professionals. Infusion of government funding into industry co-supported university training programs could bring a transformational opportunity for preparing the needed semiconductor workforce.

There are regional examples of university-based industry consortia that incorporate broader workforce training programs. The NY CREATES' 300mm pilot facilities in Albany, New York maintains technician and engineer training programs to support regional semiconductor employers (chip manufacturers, equipment manufacturers, materials suppliers, etc.) leveraging access to state-of-the-art semiconductor processing tools. Similarly, the National Science Foundation (NSF) supported Micro Nano Technology Education Center supports a Business and Industry Leadership Team which provides industry members a platform to help shape technician training to meet their needs<sup>20</sup>. These are models that can be scaled regionally and, potentially, nationally, using a hub-and spoke approach. To reduce expenses and maximize impact in setting up of such training

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<sup>19</sup> <https://www.src.org/about/>

<sup>20</sup> <https://micronanoeducation.org/industry/bilt-team>

programs nationally, a set of 200mm facilities should be set up at few easy to access universities nationwide to allow for hands-on technical training.

There are several examples of partnerships that go beyond the semiconductor industry that can be leveraged to meet anticipated needs. OneTen<sup>21</sup> is a coalition of employers, community partners and talent developers focused on a skills-first approach and focusing on competencies to close the opportunity gap for Black individuals. P-TECH<sup>22</sup> combines expertise of public and private institutions with government support to bring together more than 600 industry partners in accelerating the transition from high-school to professional careers in industry.

In addition, examples of governments convening industry participation in setting national standards such as demonstrated in the NIST National Initiative for Cybersecurity Education<sup>23</sup> and the European Skills Agenda<sup>24</sup> demonstrates the important role that government can play in catalyzing employer partnership.

### Question 3: Apprenticeships

3. What types of apprenticeship programs or existing partnerships involving workforce development issues in the semiconductor sector should the Department be aware of?

**Response:**

#### **Apprenticeship Programs**

IBM's [New Collar](#) (technical and soft skills) training programs were developed to allow students to follow non-traditional paths into productive industry employment and includes a Registered Apprenticeship Program. By the end of 2021, IBM had over 1,000 apprentices, hiring more than 90% of apprenticeship graduates as full-time employees with a 90% retention rate. For apprentices who continue their education in a school setting, these programs increase the transfer of credits

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<sup>21</sup> <https://oneten.org>

<sup>22</sup> <https://www.ptech.org>

<sup>23</sup> <https://www.nist.gov/itl/applied-cybersecurity/nice>

<sup>24</sup> <https://ec.europa.eu/social/main.jsp?catId=1223&langId=en>



from the apprenticeship training programs, with validation by the American Council of Education<sup>25</sup>. IBM has teamed with the Consumer Technology Association (CTA) to create the CTA Apprenticeship Coalition to provide frameworks, playbooks, and guidance for others to create or expand their own apprenticeship programs.

Other notable programs are those of the SEMI Foundation<sup>26</sup> partnering with academia and industry to widen the use of apprenticeship programs through such programs as the SEMI Career and Apprenticeship Network (SCAN).

GlobalFoundries, in partnership with SEMI, the National Institute for Innovation and Technology (NIIT) and New York State's Center for Economic Growth, has announced a maintenance technician apprenticeship program with SUNY. This includes customized training for semiconductor technicians at SUNY community colleges, and a parallel apprentice program at the GlobalFoundries chip fab in Essex Junction, VT. Initiated in 2021, this program takes aim at the skilled technical workforce that typically enters with a high school diploma or associate's degree. Government support for developing and expanding these networks could help to rapidly scale such programs.

### **Workforce Development Programs**

**P-TECH**<sup>27</sup> was created through partnerships that combined the expertise of public and private institutions with government support. Students complete high school and college coursework concurrently –at no cost. P-TECH was designed with two goals: 1) Address the global “skills gap” and strengthen regional economies by building a workforce with the skills required for new-collar jobs; 2) Provide underserved youth with an innovative education opportunity and direct pathways to college and career readiness. P-TECH Industry Partners enable students to participate in a range of workplace experiences, like such as internships and apprenticeships, that support student completion of their two-year postsecondary degree and prepare them to either continue their education or begin entry-level careers.

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<sup>25</sup> <https://www.acenet.edu>

<sup>26</sup> <https://www.semi.org>

<sup>27</sup> <https://www.ptech.org>

**Tech Re-Entry** and **Return to Work** programs address another common barrier –a break in work history. These programs target talented technical professionals looking to restart their careers, such as caregivers who temporarily left the workforce, and veterans. Participants use project-based assignments to refresh their professional and technical skills through mentorship, one-on-one training, and self-study of learning paths in their area of expertise.

Two other recent partnerships for microelectronics manufacturing workforce development serve transitioning U.S. veterans. The first is a new Certified Skills Program (CSP) with the U.S. Army entitled the VET Semiconductor Training and Experience Program (VET S.T.E.P.) in New York State. The second is the Nanomanufacturing Certificate Program (NCP), SkillBridge, with the U.S. Navy in Virginia. These programs offer semiconductor-specific training and, in the case of VET S.T.E.P., hands-on internship experience in semiconductor companies to military personnel transitioning out of service. Both programs are quite new and are the only CSP/SkillBridge programs that focus on semiconductor manufacturing. These partnerships are available to transitioning military service members from across the U.S. and are excellent candidates for expansion and scaling across the U.S.

**Question 3a:** What role can unionized labor play in worker training and workforce development, including for economically disadvantaged individuals?

**Response:**

American Semiconductor Innovation Coalition (ASIC) elects not to answer this question.

#### **Question 4: Education Through-put**

4. What have been successful mechanisms used by employers in the semiconductor sector to work with local high schools, career and technical education programs, community colleges, or universities to recruit and train workers?

**Response:**

The P-TECH<sup>28</sup> program is an outstanding example of accelerating the transition from high-school to jobs across a broad range of industries. With several hundred companies and over 200 schools in the U.S., P-TECH is a proven model to engage students early and achieve a high conversion rate to jobs in industry. Apprenticeship programs that are reviewed by the American Council on Education and awarded college credit hours also help to bridge between community colleges and industry and accelerate the transition from classroom to workforce.

A prime example is the HFM BOCES PTECH in Johnstown, New York, which partners Partnering with Fulton Montgomery Community College (FMCC). students are provided a path to graduate with a degree in electrical engineering technology from FMCC – a program designed specifically to support regional semiconductor ‘fab’ facilities. While this is a perfect example of industry partnering with high schools and community colleges, a key challenge is the lack of widespread engagement with middle school and high school students regarding career pathways in the U.S. semiconductor industry. To drive more enrollment in programs such as the HFM-BOCES PTECH it is essential to have greater awareness of the highly rewarding and financially beneficial jobs that the semiconductor industry provides.

In addition, individual school districts have partnered with regional semiconductor employers to help develop customized career technical education (CTE) programs – an example is Mohonasen Central School District’s Engineering CTE program in engineering (Emerging Technologies/CTE Engineering - Mohonasen Central School District, Rotterdam, New York: Mohonasen Central School District, Rotterdam, New York). Designed in collaboration with GlobalFoundries and SUNY, this program has been designed to transition high school students directly to industry. Problem-based learning, as successfully implemented in programs like such as at Springfield Technical Community College (STCC), or with classroom projects related to solving industry problems through a work and learn program, can also serve as a good model.

In the semiconductor industry, hands-on training using equipment and design tools is an essential component of being job-ready. Providing access to these through a network of educational

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<sup>28</sup> <https://www.ptech.org>

institutions is an important element of bridging between these educational institutions and industry. The community college and high school, and university programs detailed above have been successful, in large part, because of substantial capital investment in hands-on lab facilities. Without such investments – which are beyond most educational organizations means – the programs are extremely limited in their capabilities. Regional solutions to this challenge have incorporated ‘shared use’ facilities. The NY CREATES’ 300mm pilot facility in Albany, New York, is one example where high schools and colleges can leverage cutting edge semiconductor equipment or customized bench-top equipment to provide hands-on access to their students. Massachusetts has taken a similar tack in partnership with AIM Photonics, a U.S. Manufacturing Innovation Institute through establishment of the Lab for Education and Application of Prototypes<sup>29</sup> (LEAP). Spread across five universities, colleges and community colleges in Massachusetts, the LEAP centers offer hands-on access to advanced electronic-photonic characterization equipment. Cornell Nanoscale Science and Technology Facility (CNF) has developed effective training procedures on hundreds of state-of-the-art nanofabrication equipment that provides students and industry users real-world experience that will prepare them to be the next generation of leaders in technology and science. As a National Science Foundation (NSF) supported center, CNF hosts Research Experience for Undergraduates (REU) students during summers and runs an international REU program with a partner in Japan. The CNF Fellows program supports graduate students who develop new process methods and introduce new capabilities that are shared with all users, thereby lowering the barrier of entry for students and staff to gain new skills in this field.

There are some examples of similar initiatives regarding semiconductor design software to spur the training of chip designers – a critical component of the U.S. semiconductor workforce. AIM Photonics, mentioned above, engages incumbent workers and college students in free or low-cost courses to train participants in the use of design software ‘tools’ using open-source for electronic-photonic technologies. These courses allow students to submit designs for fabrication and testing at the NY CREATES’ 300mm pilot facility in Albany, New York. It is resource limited, however, and requires substantial scale-up both in capacity and scope.

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<sup>29</sup> <https://www.aimphotonics.com/projects>

A similar initiative has been undertaken by Google in collaboration with SkyWater Technology and Efabless to promote open-source design capability and fabrication on a fee-for-service basis for older chip technologies. To date, over 200 tapeouts on five multi-project wafer runs have been made; the program has engaged high-schoolers and large commercial companies alike. For education and training, an even more effective model could utilize university-based 300mm and 200mm silicon facilities where students from colleges and universities from across the U.S. can gain access to ‘chip’ design software and submit designs for fabrication and testing as part of college or university-based coursework.

Another example of an industry partnership with local community colleges and universities, is the collaboration of Cadence with North Carolina State University and the “INTERACTIVE Education in Electronic Sensing, Communication and Warfare” program. INTERACT is an innovative, experiential STEM program designed to provide Naval personnel with the technical background and skills needed for future conflicts where control and understanding of the electromagnetic spectrum and systems is essential. The program also will engage and motivate young sailors, high-school and undergraduate (UG) students in their career trajectories into STEM and electronics and electrical engineering through four program activities: (i) a digital platform for interactive training anywhere in the world, (ii) ten onsite workshops at underrepresented universities and Navy-related sites, (iii) two one-week in-residence workshops hosted at North Carolina State for Naval ROTC midshipmen, and (iv) training of U.S. citizen UGs through the development and testing of the workshop material. At the core of INTERACT is a unique systems and hands-on experiential learning approach. INTERACT will integrate Cadence commercial-grade computer-aided design tools, low-cost measurement devices and a lab-in-a-kit so that participants are able to learn through online digital media and then design, build (by hand), and test the foundational building blocks of many of the Navy’s electronic sensing and communication systems.

Another successful and sustainable public-private partnership program with high school students is the Microsoft TEALS (Technology Education and Literacy in Schools) Computer Science (CS) program. Over the past decade, TEALS has taught 85,000 high school students in over 3,000+ classes in 1,000+ high schools. In addition, hundreds of teachers are now teaching CS and advanced placement CS on their own and, as a result, students scored 5-10% above the national average every year in Advanced Placement (AP) CS exams. The program has attracted many

volunteers, providing \$165,000,000+ in value of services. This program has partnered with schools (>50% Title I, 20% rural) in underserved communities, reaching a diverse set of students (33% underrepresented minorities, 38-50% female students).

Workforce development requires a combination of training and education where the former can be targeted towards apprenticeship while the latter on a more long-term strategy for creating future semiconductor technology leaders. It is important that universities collectively develop a cohesive plan working closely with industry that includes professional development courses for training practicing engineers, hands-on training of skilled technical workers at technical high schools and two-year colleges, and the development of leading-edge semiconductor technology curriculum for four year and advanced degrees that focuses on emerging technologies. Focusing on emerging technologies can create the excitement amongst K-12 students to pursue careers and an opportunity to drive education through research to maintain U.S. leadership.

#### **Question 5: Women & Minorities (& Veterans)**

5. Are there any current or planned initiatives in the semiconductor sector to strengthen and expand the recruitment of women and underrepresented minorities, including promotion of such careers at K-12 levels?

#### **Response:**

**K-12:** Currently, there are local community-based initiatives to attract students in K-12 such as on-site school visits, Lego robotics camps, and week-long summer camps at industry sites (e.g., Girls Go Tech-Know at IBM) and universities in attempts to build a pipeline of students interested in STEM education and semiconductor technology. There are also programs for high school students that promote “innovative project-based learning,” focused on advanced manufacturing and business tools (e.g., [SparkAlpha](#)) that can be replicated and scaled more broadly. Another example of note is MIT’s Initiative for Knowledge and Innovation in Manufacturing (IKIM) that currently offers education and workforce development STEM products for the entire workforce supply chain including learners from K-12, two-year community colleges, four-year colleges (undergraduates), research universities (undergraduate and graduate), as well as incumbent

employees. These offerings are in the various formats such as: bootcamps and workshops, summer academy, technician training certificates, internships, virtual manufacturing labs, augmented- and virtual-reality manufacturing tool training, and educational videos for K-12 awareness.

Another successful program is the Microsoft TEALS (Technology Education and Literacy in Schools) Computer Science (CS) program that has taught 85,000 high school students in over 3,000+ classes in 1,000+ high schools. In addition, hundreds of teachers are now teaching CS and advanced placement CS on their own and, as a result, students scored 5-10% above the national average every year in Advanced Placement (AP) CS exams. This program has partnered with schools (>50% Title I, 20% rural) in underserved communities, reaching a diverse set of students (33% underrepresented minorities, 38-50% female students).

Expansion of efforts mentioned above to build awareness of the critical role of microelectronics in society and the environment in the K-12 levels is necessary to generate more interest at a young age and motivate more to enter microelectronics careers in the future.

**Women, underrepresented minorities, and veterans:** Active recruitment of women into the semiconductor sector is done through the student pipeline of graduate and undergraduate students established, for example, through the Semiconductor Research Corporation<sup>30</sup>, through multiple federal and state agencies, and through career fairs at diversity conferences such as the Society of Women Engineers<sup>31</sup> and Grace Hopper Conference<sup>32</sup>. The recruitment of undergraduate underrepresented minority students occurs at career fairs at various diversity conferences such as Society of Hispanic Professional Engineers<sup>33</sup>, National Society of Black Engineers<sup>34</sup>, Tapia<sup>35</sup>, and AISES<sup>36</sup> to name a few. There are success stories, for example, using these mechanisms and with a dedicated effort, at Cornell University, for example, half of all entering undergraduate engineers are women.

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<sup>30</sup> [www.src.org](http://www.src.org)

<sup>31</sup> [www.swe.org](http://www.swe.org)

<sup>32</sup> <https://ghc.anitab.org/>

<sup>33</sup> [www.shpe.org](http://www.shpe.org)

<sup>34</sup> [www.nsbe.org](http://www.nsbe.org)

<sup>35</sup> <https://tapiaconference.cmd-it.org/>

<sup>36</sup> [www.aises.org](http://www.aises.org)

To expand the recruitment of veterans and underrepresented minorities (URM), we need to create more Work-Based Learning (WBL) programs and deploy programs like the New Silicon Initiative (NSI) - designed to prepare students for careers in hardware engineering and silicon chip design – at MSIs. The National Academies of Sciences, Engineering, and Medicine, has determined that MSIs are uniquely positioned to become a large national resource for STEM talent, given that population demographics are in transition, and MSI’s currently produce 20% of STEM undergraduate degrees<sup>37</sup>. Therefore, it is of the utmost importance that MSIs develop a strong core competency in silicon design and technology to ensure full participation in the workforce at all levels of education (non-degree, two-year, BS, MS, PhD).

MSIs have been systemically underfunded: MSI students are more likely to come from low-income backgrounds, and are, therefore, more likely to suffer financial hardship. On average, Black and African American students accrue debt at twice the rate of their majority peers: undergraduate debt of \$22,720 and a graduate debt of \$44,965, as opposed to \$10, 863 and \$24,036<sup>38</sup>. Therefore, substantial long-term investments are needed to promote, sustain, and advance their success at both undergraduate and graduate levels. Consequently, the National Academies of Sciences, Engineering, and Medicine, emphasizes intentionality – “a calculated and coordinated method of engagement, by institutions, agencies, organizations, and private investors, to effectively meet the needs of a designated population within a given higher education institution” – translating into initiatives and practices that meet student needs, academically and financially, in a manner that promotes greater academic achievement and self-confidence<sup>39</sup>.

There must be both Pre-employment training, education, and supportive services that position the students for positive field experiences must be created to help students adjust to the cultural changes, new locations, and climate in the work environment. Many underrepresented students leave home for the first time to go directly to college, have never flown, are not accustomed to eating different foods, are not privy to etiquette outside of their environments, or even to being the only “one”; oftentimes, this results in culture shock. Thus, programs must include cultural competency for the students, faculty, employees, and other stakeholders such that the new

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<sup>37</sup> <https://www.nap.edu/resource/25257/interactive/>

<sup>38</sup> <https://www.nsf.gov/statistics/doctorates/>

<sup>39</sup> <https://www.nap.edu/resource/25257/interactive/>



environments openly address bias, stereotyping, and cultural neglect to create practical assimilation into the work environment. Moreover, these new experiences should include access to tools, knowledge of technologies, exposure to experts, and culturally competent mentors. Adequately transitioning women and underrepresented populations into semiconductor careers will require incentive programs that include MSIs and HBCUs, and expand access to technology, promote exchange of faculty and content experts, and provide on-site summer research experiences, mentor-mentee relationships, and accountability for all stakeholders.

Opening the pipeline aperture for workers who do not have an undergraduate degree is critical if the skills gap is to be met. This requires investing in the non-degree workforce so that they have the KSA's (Knowledge, Skills and Abilities) to be successful in these jobs. An example of this is OneTen<sup>40</sup>, a coalition dedicated to upskilling, hiring, and promoting one million Black Americans over the next 10 years into family-sustaining jobs with opportunities for advancement.

In partnership with the Semiconductor Research Corporation (SRC), an Undergraduate Research Program (URP) was created that provides a stipend to students for performing undergraduate research at their university. This program provides an early Research experience to undergraduates who may be considering the pursuit of an advanced degree in fields relevant to the semiconductor industry. Texas Instruments, Intel, Siemens, and IBM sponsor undergraduate students, with a focus on recruiting women and minorities for internships and regular, full-time employment after graduation. Since program inception in 2019, >165 students have been named SRC-URP scholars. Additionally, there are other such examples such as the NSF REU<sup>41</sup> programs and other industry funded programs at institutions of note, like the Summer Engineering Institute<sup>42</sup> at Georgia Tech for rising 11<sup>th</sup>- and 12<sup>th</sup>-graders offering basic engineering and computer science techniques and hands-on experience to solve real-world engineering programs. The NSTC infrastructure can provide the needed coordination and communication among the various levels of the engineering education system to boost the overall number of minority engineering undergraduate, graduate, and postgraduate students and faculty in U.S. colleges and universities.

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<sup>40</sup> <https://oneten.org>

<sup>41</sup> <https://www.nsfetap.org/programs>

<sup>42</sup> <https://ceed.gatech.edu/summer-engineering-institute>

In addition, a few high-tech companies have also sponsored the National GEM Consortium<sup>43</sup> whose mission since its inception has been to increase the participation of underrepresented groups (African Americans, American Indians, and Hispanic Americans) at the master's and doctoral levels in engineering and science. At the undergraduate level, the National Action Council for Minorities in Engineering<sup>44</sup> (NACME) is the largest provider of college scholarships for underrepresented minorities pursuing degrees at schools of engineering. Expanding participation in these programs can offer an expanded opportunity to build a student pipeline along with mentorship and internships for the sponsored students.

The SEMI Foundation<sup>45</sup> provides robust resources to promote practices that industries can leverage to hire, retain, and promote more women, people of color and veterans. These nationwide resources are meant to complement the work being done at the community level. The SEMI foundation runs a nationwide Industry Image & Awareness Campaign to address the relative invisibility of the sector to workers in hopes that it will intrigue significantly more students, veterans and women returning to work to explore opportunities in the industry.

**Students in rural communities:** Another very under-represented group in R1 (doctoral) engineering programs is students from rural communities (total U.S. population of ~60 million). Current programs do not address outreach and education for those (vast) regions of the country. An effective outreach vehicle is 4-H that has a program in each county in every state in the union with a focus on STEM activities as a core of its mission. Cornell University, a land grant school and home to the local 4-H, has established an outreach activity through Cornell Nanoscale Science and Technology Facility (CNF), its NSF-supported nanofabrication facility, teaching nanoscience and electronic materials, and providing science and engineering activities to interest students from largely rural communities. These activities are shared across the country, creating an enormous multiplier effect, and additional efforts should be directed to this community.

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<sup>43</sup> <https://www.gemfellowship.org>

<sup>44</sup> <https://www.nacme.org/>

<sup>45</sup> <https://www.semi.org>

### Question 6: H1-B

6. To what extent, and for what occupations, do organizations in the semiconductor sector use the H1-B Program to fill positions?

#### Response:

From the semiconductor industry perspective, we recognize there is a shortage of domestic talent with specific high skills and advanced degrees ranging from materials science, electrical engineering, physics, or chemistry. While upcoming efforts by the U.S. government, academia, and industry are intended to build a strong domestic pipeline of talent, in the short term the U.S. semiconductor technology sector continues to look to foreign nationals under the H1-B category to supplement the talent pool.

### Question 7: Ensuring Semiconductor Growth

7. Are there opportunities to design the semiconductor incentive program to ensure that worker skills shortages do not hinder companies from expanding operations?

#### Response:

With 7% attrition and continuous re-training, the cost of workforce development cost for the 300,000- member strong semiconductor industry is greater than \$5 billion per year. The semiconductor incentive program should be designed to provide programs for retraining and upskilling workers that already have the relevant foundational skills. The incentive program also needs to find opportunities to make the jobs in those expanded operations competitive in pay and benefits compared to other industries that are competing for similar talent. Using the incentive program to also ensure that the semiconductor workforce is recognized for the vital economic engine that it is enabling, will instill a sense of pride in these occupations.

As an example, many critical areas in modern semiconductor manufacturing operations require software and data analytics skills. These include the need to apply intelligent data mining and artificial intelligence to improve manufacturing yield, as well as the automation of equipment and

logistics in such facilities. As another example, retraining of plumbers and electricians to handle specialty services like toxic gas systems and chemical waste management, along with the appropriate certification framework, will allow the expanded operations to rapidly draw upon local skilled workers. Drawing upon the rich experience of veterans with engineering skills in handling complex equipment through retraining and certification will also enable expanded operations. Taking advantage of recently approved U.S. DoD CSP/SkillBridge programs such as the VET Semiconductor Training and Experience Program (VET S.T.E.P.) with the U.S. Army in New York State or the Nanomanufacturing Certificate Program SkillBridge with the U.S. Navy in Virginia could be excellent incentive programs to engage the more than 200,000 military service members that transition to the civilian workforce every year.

Graduate students with different expertise can also be incentivized to quickly shift career paths to meet the needs of an expanded semiconductor industry and incentive program recipients. These are just some of the opportunities to design the incentive program in such a way that industry can collaborate with training institutions to rapidly address the workforce challenges of expanding operations.

## ADDITIONAL POINTS FOR CONSIDERATION

- 1. Preparation and delivery of curriculum:** The content of semiconductor curriculum needs to be modernized to train the workforce in the latest techniques that include automation and the application of new technologies such as AI to semiconductor design and manufacturing. Lessons can be learned from education initiatives undertaken to expand the fledgling workforce in quantum computing using open-source textbooks, access to quantum computing resources, and programming bootcamps. In addition to content itself, engaging a new generation of educators and students with the latest compelling modes of content delivery including multimedia and immersive technologies will help to attract and retain them. Resources need to be directed to incentivize institutions to modernize educational content and content delivery aligned with the needs of the semiconductor industry. Curriculum modernization is underway as part of the SEMI Career and Apprenticeship Network (SCAN). It is also underway as part of the – the National Institute for Innovation and Technology (NIIT)

National Talent Hub which provides educational institutions with direct access to the skills and competencies needed by the U.S. semiconductor industry. Both initiatives require funding for rapid scaling nationwide. There must be incentives to direct higher-education faculty renewal and hiring towards the semiconductor sector, and the supports to ensure success of young faculty in this area.

- 2. Effective and scalable outreach programs to students at all levels:** While the awarding of academic STEM degrees and certificates have been steadily increasing in the U.S. in recent years, the fraction of those degrees leading to careers in the semiconductor industry have been falling. Scalable semiconductor science and technology programs that target young students at key decision points in the education pipeline are essential so that students understand the variety and positive social impact of careers in the U.S. semiconductor industry. Chip design and testing camps (akin to ‘hack-a-thons for coding), engineer shadowing, teacher ‘externships’ and targeted semiconductor technology fellowships at 2-yr colleges, 4-yr colleges and graduate research universities are a few key elements that need to be developed and scaled to promote the U.S. semiconductor workforce to ensure U.S leadership in microelectronic technologies for decades to come. A key factor in the successful development of a semiconductor workforce is access, enthusiasm, and development of an engineering identity at all levels of participation (K-12, non-degree, BS, MS, PhD), and approaches such as these can help to address this.
  
- 3. Access to tools, silicon, and validation:** Wide access on a national scale could be provided through the creation of a national innovation and design center comprised composed of national cloud-based computing facilities to host training material, tutorials, open-source and commercial CAD (Computer-aided Design) tools/Process Design Kits (PDKs), and provide computing resources. Open access at an early stage and community collaboration, leads to improved innovative solutions. The value of open-source PDKs/IP and the Hackathon/Bootcamp model in semi-conductor workforce development is now acknowledged by the recently launched IEEE Solid-State Circuits Society (SSCS) Platform for IC Design Outreach (PICO) and associated open-source ASIC competition<sup>46</sup>. PDKs and IPs for design

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<sup>46</sup> <https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-design-contest>

activities such as those provided by SkyWater also serve as an example. As previously mentioned, participants at all levels benefit greatly from industry-standard hands-on experience. Multi-Project Wafers (MPWs) provide a cost-effective mechanism for open-source tape-outs and a national network of post-silicon validation labs, including the auxiliary support and infrastructure (PCBs, test equipment, etc.), ensures an end-to-end experience, from initial design to bringing up and testing a chip, for the open-source community. In cases where restricted access is necessary, the cloud computing resources could be federated to provide the highest level of security for export controlled and defense related PDKs/research and open-access for other usage.

- 4. Access to advanced hardware prototyping:** Beyond the technology development on conventional silicon platforms, we need to ensure that our workforce can also be prepared to invent and scale novel semiconductor technologies. Having a facilitated and subsidized access to hands-on hardware tools is the key to developing new materials and processing platforms. Hence, the access to upgraded hardware resources spread across shared facilities at U.S. research universities, at national labs, and at other accessible hands-on semiconductor facilities is the key to making such advancements. The access to such subsidized and shared toolsets is particularly impactful when supporting the workforce that will launch new start-up ventures. We can dramatically accelerate the success of early-stage start-up companies by providing them access to tools that they need to make prototypes. Connecting start-ups with prototyping facilities at universities in this manner catalyzes the connection between talented students and commercialization of novel ideas.