Technical Memorandum

Ambature TM # 2020-03

To: Ron Kelly, CEO, Ambature Inc.

Cc: Mike Lebby, Mitchell Robson

From: Davis Hartman

Date: 03/12/2020

Re: **Post-Epi Processing of Tri-Layer a-axis Grown JJ Wafer Substrates**

Ron,

The purpose of this memo is to give the reader a cursory description of the fabrication process occurring as we develop our tri-layer a-axis oriented Josephson Junction device. We will describe this process in a very general way. It is not intended, nor will it be a detailed description of the fabrication of a tri-layer J-J device. It should be kept in mind that since the device is still in the early "exploratory development" phase, the fabrication process is iterative, involving experimental measurement and device evaluation steps, with design evolution occurring as part of this development.

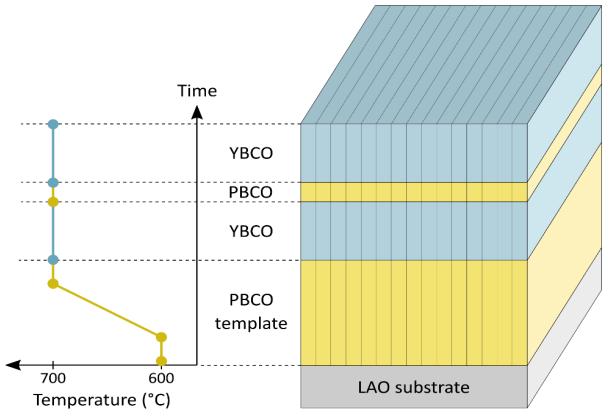

Figure 1: Tri-layer a-axis layout on LAO substrate.

Currently, we are involved in the exploratory development of the required tri-layer YBCO/PBCO/YBCO thin films, deposited onto an appropriate three-inch substrate material (currently LAO). Figure 1 shows the structure of our tri-layer film deposition and the epitaxial growth profile. The figure depicts the a-axis oriented vertical growth. To experimentally evaluate the performance of this epitaxial structure as a superconducting device, we must be able to measure current and voltage (as well as apply voltage in some instances) at the layers without damaging them. Traditionally, in integrated circuit fabrication, we accomplish this by removing and reshaping parts of the substrate via wet chemistry and photolithography. Material is

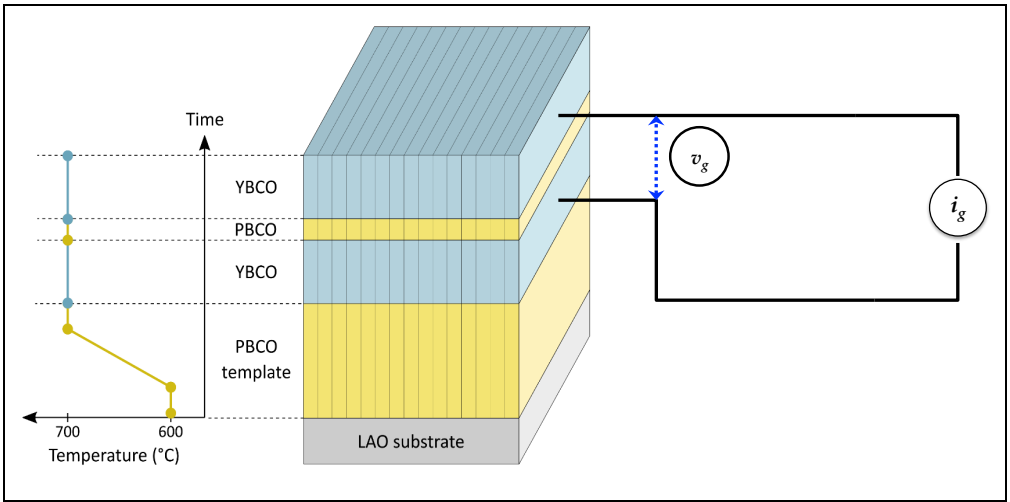

Figure 2: Tri-layer a-axis layout on LAO substrate, now showing the voltage and current access points needed to test and evaluate the device.

chemically removed and replaced with metal, photoresist and the like, to form "probe points", i.e., pads where electrical contact can be made.

Ambature's objective in the current a-axis J-J project is to demonstrate experimentally the functionality of a Josephson Junction, built on a-axis oriented YBCO. For this first phase (successful growth of a tri-layer YBCO/PBCO/YBCO), we are focusing on the goal of experimentally demonstrating the DC-Josephson effect on our a-axis films. We will do this by generating an *i-v* characteristic curve of the a-axis grown substrate and by measuring, directly from the same i-v curve, the critical current of the device. Figure 2 shows what we must measure and where it lies in the substrate epitaxy. Right now it looks like we can evaluate the functional behavior of the tri-layer structure by gaining access to the two YBCO layers, without needing to directly access the insulating PBCO layer. Later in the development process that will be needed, but for now it is not. At this point in our J-J development, we are ready to chemically process the grown three-inch wafer to form the electrical contacts needed to experimentally evaluate the device at temperature.

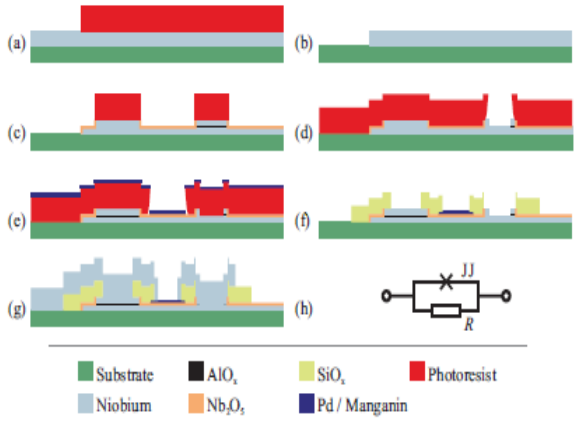

Figure 3: LTS Tri-layer fabrication process. Pictorial example of the photolithography and chemical etching process gains access to inaccessible buried layers in a thin film stack.

Figure 3 depicts what we mean by "chemical processing" of the wafer. The figure, while not in any way technically related to our structure, helps to give the reader an understanding of how photolithography and wet chemistry can be implemented to gain access to and create physical structure to the IC.

Regards,

Davis Hartman