Opening New Superconductivity Markets through Cost Reduction via a-axis Epitaxial Growth and Economies of Scale

A White Paper Offered by

Ambature Inc.

Ron Kelly CEO

November 1, 2016

1. Executive Summary

High Temperature Superconductivity (HTS) is and has been a promising technology for a number of signal processing, communications and industrial applications. However, success of HTS in the marketplace is and has been severely hindered by the complexity (and resulting high cost) of the technology, particularly when device processing is considered. Current HTS materials (like YBCO) are ceramics (unlike LTS materials, which are metals) with anisotropic transport properties. As a result, even the most basic HTS device, the Josephson Junction, requires processing technology that is far too complex to be cost effective in the marketplace. The HTS industry is stuck in a technology cul-de-sac that cries for a breakthrough.

We offer that breakthrough. Using an unorthodox epitaxial growth strategy called “a-axis growth”, we greatly simplify the HTS device processing challenge. With this strategy, we can take advantage of the economies of scale that accompany high volume device manufacturing on large starting wafers. The result will be a significant cost-performance breakthrough and emergent opportunities for new markets.

2. Introduction; A Breakthrough is needed

Since the first discovery of high temperature superconductivity in 1986[1], the search for new High Temperature Superconductor (HTS) materials has been impaired by the unanticipated complexity of the problem. HTS materials are different than LTS (Low Temperature Superconductor) materials. They are mostly ceramics with anisotropic crystal structures. In contrast with LTS materials, the transport dynamics of HTS materials are still subject to intense debate. Despite some success at experimentally characterizing the Fermi surface of new HTS materials[2], the dynamics of the HTS superconducting phase transition is still a mystery.

Because of this complexity, fabrication of even the most basic HTS device, the Josephson Junction (J-J), has posed a formidable growth and processing challenge. To date, "The equivalent of the classical tri-layer junction structure, which is commonly fabricated with LTS, has not yet been reproduced with HTS" [3].

Early on in the evolution of HTS development, attempts to build an effective tri-layer J-J structure using a-axis deposition/growth techniques were deferred in favor of more complex device processing methods, because the required tri-layer growth dynamics were so very challenging. Other structures, including micro-bridge junctions, point contact junctions, ramp style junctions and tilt or twist grain-boundary junctions, were pursued instead. Even today, literature reports on HTS J-Js are based on these very complex structures.

While there has been progress at fabricating these alternative J-J structures, no significant breakthroughs have yet occurred. These structures require complex growth, deposition and processing approaches that limit the integration of many devices on a chip because, using these approaches, the device structure must be defined at the epitaxial level. Without the ability to integrate many devices on a chip, the cost at the product level is too high and high volume markets are unreachable. *We need a breakthrough.*

[1] Bednorz, J. G. , K. A. Muller, Z Phys. B **64**, pg. 189 (186)

[2] Paglione, J., R. L. Greene, "High-temperature superconductivity in iron-based materials", *Center for Nanophysics and Advanced Materials, Department of Physics, University of Maryland, College Park, MD 20742, 2010.*

[3] Schrieffer, J.R., J.S. Brooks, Handbook of High Temperature Superconductivity, pp. 20-21.

3. The Breakthrough

A breakthrough is needed to enable the fabrication of HTS tri-layer vertically conducting Josephson Junctions, at high volume and with high yield. Such a breakthrough can change market dynamics for HTS. With a standardized HTS tri-layer J-J process, affordable devices and subsystems on a chip will begin to emerge. Medical imaging devices and systems, produced in high volume, will compete with traditional bulk RF components, offering higher performance at reduced size, weight and power (SWaP) and at competitive or even lower price. Multi-channel signal processing system architectures used in driverless cars and industrial control systems could benefit from higher dynamic range offered by HTS based sensors and quantizers.

Our breakthrough begins at the choice of substrate material and runs through the thin film deposition/growth and continues through device processing. Epitaxial growth of HTS materials on large silicon-compatible substrates will require a multiple series of "buffer layers" situated between the host substrate and the first functional layer. These layers will reduce stress induced by lattice mismatch, establishing a basis for device reliability. This wafer/buffer layer structure constitutes a starting wafer for HTS processing and fabricating complex high performance superconducting circuits with high yield, large volume devices at reduced cost and high performance.

When an HTS tri-layer J-J is reproducibly built from known superconducting materials using a well-established fabrication platform, several significant benefits will result. Initially, we will acquire a firm understanding of the functions of the Josephson Junction in an HTS materials venue. We will be able to directly measure the energy gap, the critical current of the device, observe and measure tunneling and flux quantization in the device and relate it to the quality of our films. This understanding will spawn new invention on uses and applications of the J-J. We will develop expertise on tri-layer J-J design and fabrication.

A valuable but less obvious benefit will emerge as we develop these devices. The J-J itself will find use, not only as a tool to develop products, but also as a scientific probe into the HTS mechanism itself. This advantage will accelerate our learning curve toward developing superior devices.

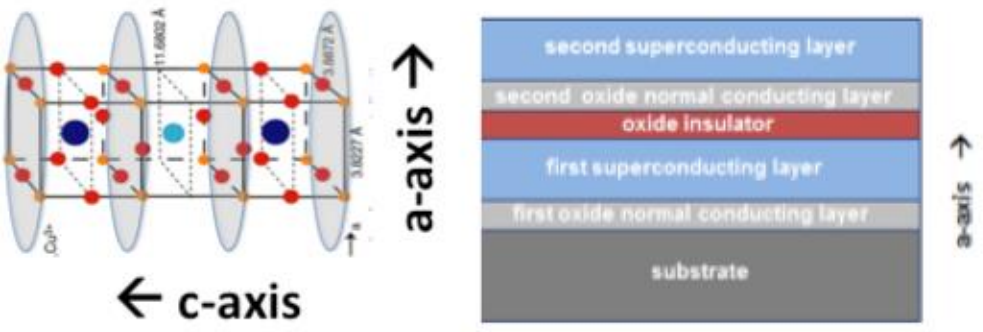

Figure 1: Simplified view of the epitaxial layers needed to implement a tri-layer Josephson Junction. Not included in the diagram are a series of buffer layers between the substrate and the first oxide normal conducting layer.

4. The a-axis Growth Alternative

The Josephson Junction is as basic and necessary to superconductivity as the transistor is to integrated circuits. Development of the tri-layer J-J will enable integrated HTS just as the transistor enabled huge opportunities brought by VLSI, and a-axis growth is a key enabler.

YBCO is an anisotropic superconductor. Super-currents can flow in its crystallographic a-axis and b-axis, but not the c-axis. When a film of YBCO is grown on a substrate, nature's preferred growth orientation is along the c-axis (c.f., Figure 1). But, because there is no mechanism to support vertical currents, tri-layer Josephson Junctions cannot be produced using conventional c-axis growth kinematics. Instead, c-axis oriented J-Js must be fabricated to conduct in the horizontal plane. The complexity of these solutions is as formidable as the problem itself. Furthermore, it is not clear how many J-Js can be fabricated on a single chip with c-axis growth.

If high quality YBCO is grown with a-axis orientation on a common substrate, vertically conducting J-Js can be fabricated, in high volume and in a simple tri-layer structure using standard silicon fabrication techniques (without the need for specialized and custom tooling). The vertically conducting tri-layer structure is a scalable solution; if one J-J can be built on a chip from large wafers, the integration can be scaled from SSI (small scale integration), to MSI (medium scale integration), LSI (large scale integration) and beyond.

The approach to generate a-axis films stems from the work that Ambature has already completed using PLD (Pulsed Laser Deposition). This work involved the use of SLGO substrates to ease the lattice matching of the YBCO deposited films. Table 1 shows some

Ambature PLD a-axis growth results. These results indicate that, within the limit of measurement errors, the a-axis alignment is typically in the 90th percentile or better.

Sample Number/Type	Film thickness (Å)	a-axis orientation (%) ± 0.1 (%)	b-c plane orientation (%) ± 0.1 (%)
YBCO 1	*6,520*	*98.4*	*81.3*
YBCO 2	*6,450*	*41.3*	*72.8*
NBCO 1	*11,680*	*>98* *	*83.4*
NBCO 2	*14,300*	*95.3*	*72.9*
DBCO 1	*7,590*	*86.2*	*87.0*
DBCO 2	*7,310*	*89.1*	*91.4*
PBCO 1	*18,530*	*>98* *	*88.1*
PBCO 2	*11,120*	*88.8*	*51.4*

Table 1: Plot of measured film thicknesses and the degrees of orientation for a representative sample of a-axis grown films. Within the limit of measurement errors, the a-axis alignment is typically in the 90th percentile or better.

While PLD can produce very high quality films, the technique does not allow for fine control of layer thicknesses (which are needed to develop sandwich epitaxial layer devices as are found in Josephson Junctions (see Figure 1). In order to address the layer quality and thickness issue, there are two emerging techniques that can address this challenge: Atomic Layer Epitaxy (ALE) and Molecular Beam Epitaxy MBE. Both of these techniques generate high quality epitaxial layers, and both can produce excellent thickness control. The advantage of ALE over MBE is that the layer thickness control is self-limiting, thereby creating a natural thickness control technique.

Table 2 (below) lists the development tasks that will be undertaken in addressing this approach.

1	Review Ambature's past results on PLD grown materials on SLGO
2	Choose a substrate/template technology that can scale or is available today at 100mm. This may well be silicon carbide. It may also be silicon or sapphire.
3	Focus on effective buffer layer technology to provide high quality YBCO onto the substrate (assume SiC for the basis of this argument).
4	Demonstrate a thin high quality YBCO epitaxial layer on the YBCO buffer layer and confirm using typical material diagnosis techniques (AFM, XRD etc.)
5	Demonstrate a thin high quality NdBCO (or equivalent insulator material) that can be epitaxially grown onto the thin YBCO layer using ALE
6	Demonstrate a thin high quality YBCO layer to complete the insulator sandwich and show that the complete stack of epitaxial layers at this point are of high quality material using standard diagnosis techniques.
7	Improve wafer uniformity, and quality across the 100mm wafer so that the wafer can be subjected to fabrication of JJs
8	Develop a JJ process to fabricate the ALE based YBCO template wafer.
9	Fabricate a JJ using standard clean room fabrication equipment on 100mm wafers.
10	Test and evaluate individual JJ devices for performance
11	Initiate life testing and reliability of individual JJ devices.
12	Review and evaluate potential packages for JJ devices for customer verification and testing.

Table 2: An outline of the tasks that will be carried out in developing an a-axis grown tri-layer Josephson Junction HTS breakthrough solution.

Product Application	Product	Potential Customer(s)	Worldwide TAM
Medical Imaging Portable (MRI)	SQUID detectors to replace Faraday loops	GE, Philips, Siemens, Toshiba	$40 Billion in diagnostics
Cellular Radio	RF Filter Banks	NSN, Alcatel/Lucent, Ericcson, Motorola, Hauwei, ZTE, Samsung	$120B increasing to $500B with 5G
Digital Signal Processing	High performance ADCs, RSFQ digital circuits	Analog Devices, cirrus Logic, Intel, National Semi.	$332B

TABLE 3: Estimates of market opportunity for a-axis grown HTS technology and IP in three market segments; medical imaging, cellular radio and digital signal processing.

5. Business Opportunities

We have seen that a-axis oriented epitaxial growth of YBCO on large substrates offers new opportunities for technological insertion of HTS into thus far untapped markets. In this section we describe three such market opportunities. These are medical imaging, cellular radio base stations and digital signal processing.

Point-of Care Medical Imaging Systems (MRI)

At Ambature, we are currently exploring the use of our a-axis growth technology in MRI markets. This market is currently evolving from the large B-field (> 0.5 Tesla) multi-million dollar units to smaller, more portable "point-of-care" units that must be priced much lower and would strongly benefit from portability. These market requirements (along with size, weight and power restrictions for portability) tend to imply the use of very low polarizing B field, or perhaps even the absence of a large electro-magnet altogether. As the attached Figure 2 shows, with the use of SQUID loop detectors in place of conventional Faraday detectors in the low B-field regime, significant Signal-to-Noise Ratio (SNR) improvement can accrue. We note in passing that in the high field regime, there is no advantage to using SQUID detectors, since the sample noise dominates in this regime.

Therefore we conclude that, from a systems perspective, the use of high temperature superconducting detectors in low B-Field MRI applications is advantageous, even though the operation at 77K is less sensitive than 4K LTS operation. We further conclude that with the use of HTS rather

than low temperature superconducting solutions, the 4K cryo-environment can be altogether eliminated (further reducing size, weight and power), since low B-fields can be produced with ferro-magnets rather than superconducting magnets. These advantages allow us to focus our technology development toward a set of specifications for HTS Josephson Junction devices that are consistent with the systems picture. This is what we mean by the term "System-Driven Technology Development".

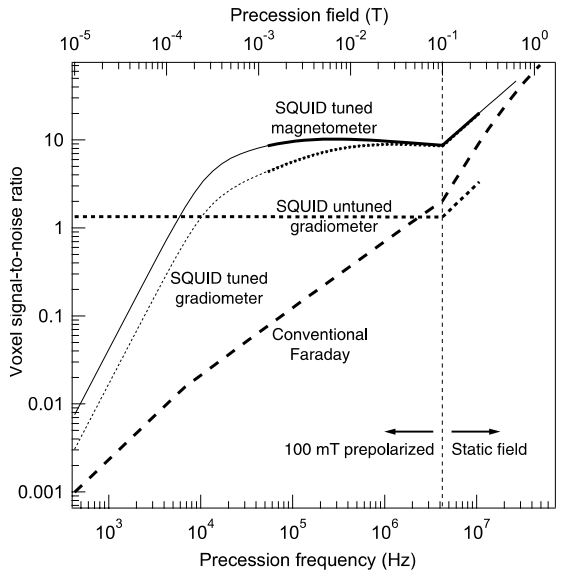

Figure 2: Low field MRI is possible when pre-polarization techniques are used.

Cellular Radio Base Stations

Cellular radio system base stations have evolved into complex bandwidth-hungry data processing centers. Bandwidth demands of social media are insatiable, with no end in sight. Thousands of incoming signals must share an overcrowded frequency spectrum with between 800 MHz and 1.9 GHz. Bandwidth efficiency needs drive the industry to pack as many signals in the allocated frequency spectrum as possible. Incoming signals are carefully filtered from each other using RF band pass filter banks. These filters must reject out-of-band signals over a relatively narrow band and over a relatively wide dynamic range. That is, the filter must be capable of simultaneously rejecting out of band signals that are very large and very small. This feature in a filter is called "selectivity". As we see in Figure 3, among the factors driving filter design, the ones driving the need for sharp filter skirts, very high Q and low insertion loss. Collectively, this suite of requirements is often referred to as "filter shape factor".

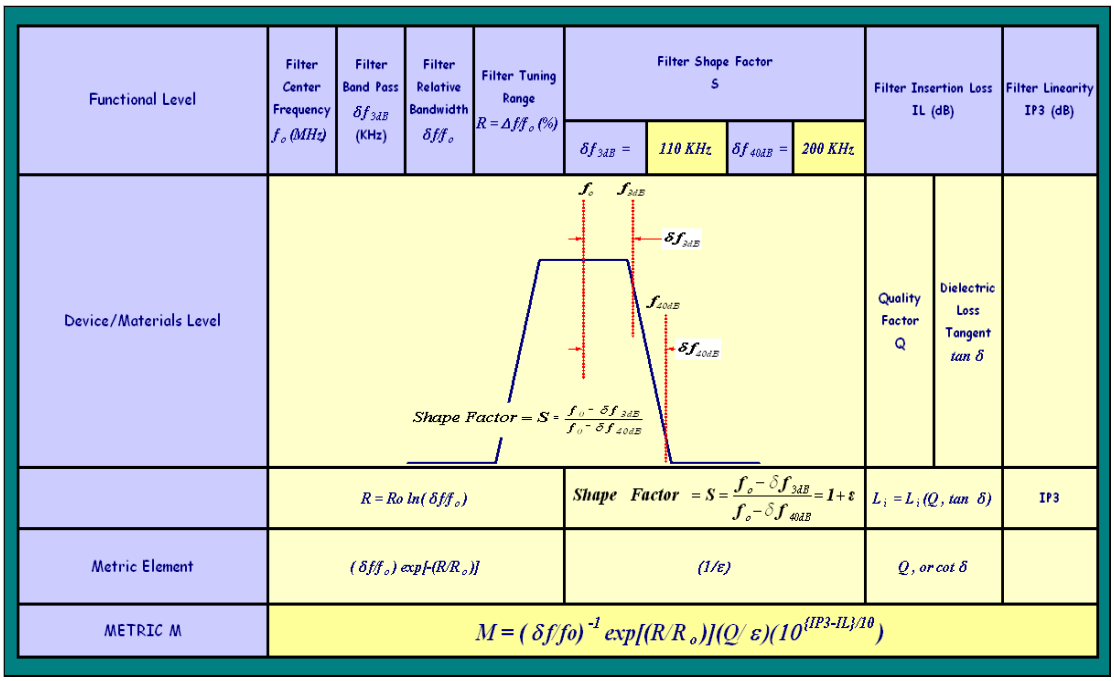

Figure 3: Cellular systems pre-select filter banks must satisfy a number of important requirements, including high selectivity (shape factor) and quality factors. These two metrics are the main reason why HTS filter banks have been implemented as pre-select filters in base station front ends.

The very high Q and low insertion losses of superconducting filters have opened a market for HTS filters in the cellular systems industry. Base stations implement HTS filter banks since c. 2003. It is expected that this trend will continue with increasing emphasis on lower cost and higher functionality. Ambature's a-axis grown materials can meet this growing need by offering higher design features through the capability to include (at reduced cost) active circuitry in the filter bank designs.

Digital Signal Processing

The world market for all digital signal processing components and modules is very large; at leas $330B and growing rapidly. All signal processing systems, from advanced analog receivers to FPGA-based data processors to sensors systems and other real-time signal processors, are continuously in need of higher performance at lower cost and with lower power consumption, so there is great opportunity for new technology insertions that can enable higher performance systems. This market, however, has already benefitted from enormous investment in silicon IC technology (R/D, design manufacturing, etc.).

To be adopted by the silicon IC industry, superconductive solutions must be viewed as a useful design tool, rather than competing with silicon. There are already some niche markets for HTS in the digital signal processing industry. It is likely that more niches

will open; particularly as new HTS materials emerge with higher critical temperature. For Ambature, the value of our IP in this area will only grow as the silicon industry progresses and as high temperature superconductivity R/D moves forward.

In general, the technical areas where our IP will grow in value are those where mixed-mode signals (that is, both analog and digital signals) must be processed. For example, low temperature superconductive analog-to-digital converters (ADCs) have already been designed and implemented by Hypres. These ten bit devices operated at a sampling rate of 20 Gsps, consuming very little power. However, the complexity of the system was very high and operation at liquid helium temperature was a factor that is difficult to overcome in the rapidly moving solution-oriented silicon IC market.

Another (related) area where HTS markets will likely grow is the use of Rapid Single Flux Quantum devices. RSFQ is a well-established means of digitizing superconducting signals for use in DSP. It is used in the ADC applications discussed earlier, as the heart of signal quantizing. An area of great promise for this application genre is in the "Advanced Receiver" field. Advanced Receivers (see Figure 4) are an architecture (related to software defined radio) where a whole suite of digital signal processing assets are connected (via a high speed switch matrix) to an array of analog and sometimes digital signals in a way that maximizes use of these assets and enables very agile processing of complex waveforms in a variety of applications.

At Ambature, we have generated a significant amount of IP in the HTS sensors and sensor systems area. This IP, when applied in the silicon DSP area, could enable new performance features. In this case, the key IP concept is means and methods for

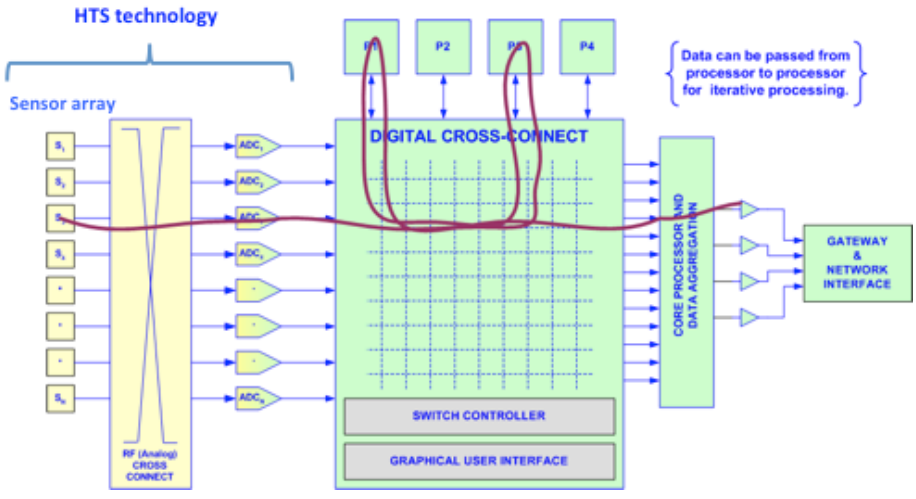

Figure 4: Application area for HTS applied to digital signal processing. Asset allocation in complex real-time digital processing systems requires agile sensors an analog-to-digital conversion.

implementing tri-layer Josephson Junction devices in LSI systems-on-a-chip.

6. Moving Forward (i.e., what we want to do and what resources would be needed)

Since the last attempts to fabricate tri-layer Josephson Junctions from a-axis grown YBCO[4], there have been significant advances in epitaxial growth technology. In atomic layer epitaxy as well as molecular beam epitaxy, controlled growth of oxide buffer layers on lattice-mismatched substrates has been achieved in materials and applications in the optoelectronic industry. With Ambature's experience in growing a-axis oriented YBCO films on lattice matched SLGO substrates and the recent advances in epitaxial growth, it is more likely that growth of YBCO on silicon compatible substrates will be successful.

We are seeking investment partners to develop the growth capability and to produce a functioning tri-layer Josephson Junction on a silicon-compatible substrate. We propose a three-pronged approach to develop the needed technology;

1. Develop a growth process for growing YBCO layers on SiC, which is a starting substrate for silicon IC processes. The growth process will employ a series of buffer layers designed to accommodate the lattice mismatch between YBCO and the host substrate (probably SiC)
2. Build a proof of concept (POC) tri-layer Josephson Junction on SiC using the growth process developed in (1) and demonstrate basic functionality (DC Josephson effect) on these devices.
3. Investigate what would be required to modify a standard CMOS IC process to operate at 77K, where HTS circuits operate.

This three-pronged approach (a-axis epitaxial growth, tri-layer J-J fabrication and low temperature CMOS process requirements) taken together could move high temperature superconductivity well into the domain of low cost high performance electronics. These three efforts are described below.

Materials/Growth

We will demonstrate, through a POC, that a-axis grown YBCO on silicon carbide substrate (or equivalent) is feasible and compatible with a standard silicon fabrication plant. Initial wafer sizes are expected to be 100mm. Further development work could increase the wafer size to 150 and 200mm.

In order to realize a POC a number of basic materials and device steps need to be accomplished. These include the design and choice of an epitaxial layer deposition tool.

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[4] Takeuchi, I., P. A. Warburton, Z. Trajanovic, C. J. Lobb, Z. W. Dong, T. Venkatesan, M. A. Bari, W. E. Booij, E. J. Tarte, and M. G. Blamire, "Fabrication of in-plane aligned a-axis oriented YBa2Cu3O7x trilayer Josephson junctions", Applied Physics Letters 69, 112 (1996).

The initial choice will likely be low pressure ALE (as per the tool kit at SUNY) where layers of YBCO would be deposited onto silicon carbide wafers.

In parallel with this work, a MBE (molecular beam epitaxy) tool will also be utilized to deposit high quality YBCO layers onto silicon carbide wafers. Both systems will operate with 100mm silicon carbide wafers. Access to a MBE reactor would be via a supplier relationship that already owns a commercial MBE reactor. This would be via a standard lease agreement.

Device Fabrication

The fabrication work of creating a-axis JJs will be via the SUNY facility in New York State. Key to the fabrication will be the use of standard process techniques that are utilized in the silicon semiconductor industry. Even though initial wafers will be grown onto 100mm substrates, the effort will be to increase the size of the wafers so that a standard line at SUNY can be used to produce CMOS compatible process techniques for a-axis JJs to operate initially at 77K. Standard process travelers will be created, along with standard CMOS PDKs (process development kits).

HTSMOS Platform Integration

The fabrication of a-axis JJs in a CMOS compatible fabrication plant will mark the first steps in creating a new and novel monolithic platform for YBCO and CMOS integration. The new platform will be entitled HTSMOS (High temperature superconductivity MOS) and will include both YBCO based a-axis JJs with standard CMOS technology, optimized for 77K temperature operation.

It is envisaged that during the project, the focus will be to produce CMOS compatible a-axis JJs not only on silicon carbide, but also on silicon wafers, so that wafer fabrication and testing can be standardized. We choose silicon carbide as the initial wafer platform since its crystalline structure offers an excellent opportunity for high quality single crystal YBCO a-axis material growth.

Testing of the wafers should be done using standardized test and probe equipment that is seen in the silicon industry. Since large format wafers are being considered, the issues of integration of the disparate technologies are eased.

Resources

REDACTED

7. Summary

Ambature offers a cost-conscious solution to the long-standing problem of untenable complexity in high temperature superconductive technology. The solution employs an unorthodox epitaxial growth approach, referred to as a-axis growth. In this approach we take on the complexity burden of a-axis epitaxial growth to relieve the severe processing burdens that accompany the much more commonly employed c-axis growth strategies.

In spite of the acknowledged subtleties associated with a-axis growth, Ambature has successfully and consistently grown YBCO on host SLGO substrates with a-axis orientation. The next logical step is to grow YBCO on larger silicon-compatible host substrates like SiC or sapphire using well-established buffer layer growth techniques developed in the photonics industry over the past thirty years. Once this growth technology is established, the fabrication of tri-layer Josephson Junction devices becomes very much attainable. This breakthrough in turn will make it possible to develop highly complex system level solutions on a chip using the tri-layer J-J as the basic building block. In like manner to the silicon IC industry, high volume, high yield production of HTS ICs will drive cost down via economies of scale. When this happens, markets for devices in the medical, industrial, communications and eventually consumer industries will be enabled.

Ambature seeks investment partners to develop the a-axis growth technology on large substrates, and to use this technology to develop a proof of concept J-J device, toward the eventual development and release of a full systems demonstrator of the a-axis grown tri-layer J-J technology.

Technical Memorandum

Ambature TM # 2020-01

To: Ron Kelly, CEO, Ambature Inc.

Cc: Michael Lebby

From: Davis H. Hartman

Date: 01/23/2020

Re: Update on 2016 White Paper: Technology Developments Influencing Ambature's Inventory of Opportunities

Ron,

Since the release of TM # 2016-01, entitled **"Opening New Superconductivity Markets through Cost Reduction via a-axis Epitaxial Growth and Economies of Scale"**, the technology landscape has evolved to a considerable extent and the impact on society is already discernable. We have been revisiting and updating the contents of our 2016 White Paper in light of progress in the semiconductor industry and cellular systems.

In the semiconductor industry, Moore's law, which reflects the incremental decrease in transistor feature size with commensurate increase in IC transistor count, continues. However, the laws of physics are imposing unmistakable limits to Moore's law. Breakthrough technology is required to support the continuing expansion of the semiconductor industry.

In the communications industry, the fifth generation (5G) cellular communications systems present a vision of the not-too-distant future that call for extended bandwidth, lower latency and greater flexibility for the user. These visions are driving technology breakthroughs to support the 5G standards.

More than ever before, the semiconductor industry and the wireless cellular industry are interlinked, driving each other toward the next generation. The future is bright for the semiconductor industry and opportunities abound for reach-out technologies like superconductivity.

In that original 2016 white paper, three technology spaces were discussed. These were,

(1) Point of care medical imaging
(2) RF/microwave filter arrays for wireless communication base stations.
(3) Digital signal processing

Since 2016, the landscape for communications, computation and medical systems has matured significantly. In this memorandum, we outline these changes and discuss how they can impact the opportunity space for High Temperature Superconductivity (HTS).

In the *semiconductor industry*, we report the findings of the IRDS (International Roadmap for Devices and Systems) working groups and IRDS technology roadmap. In particular, we describe and report on the findings of the "Beyond CMOS" working groups within IRDS. This group has been exploring and assessing merits of a number of emerging technologies, including superconductivity, that hold the potential to augment or even supplant silicon IC technology.

We report on evolutionary advances in *wireless communication systems*, driven by the semiconductor industries Fifth Generation Wireless Technology (5G), ultra-wideband modem designs, cellular communications standards efforts and continuous strides in signal processing, artificial intelligence (AI) and medical devices.

In the *medical industry*, we report on significant advances in design and prototyping of novel low B-field MRI tomography technology.

Silicon IC industry

The silicon IC industry is now more than sixty years old and it is still growing. Total global sales in 2019 for the silicon semiconductor industry were $409 B. This estimate does not include sales of the devices, components, modules and systems that are designed and built from (which exceeds $100 B per year. Since the first IC was sold in1958, total accumulated sales in the semiconductor industry now exceed $10 T.

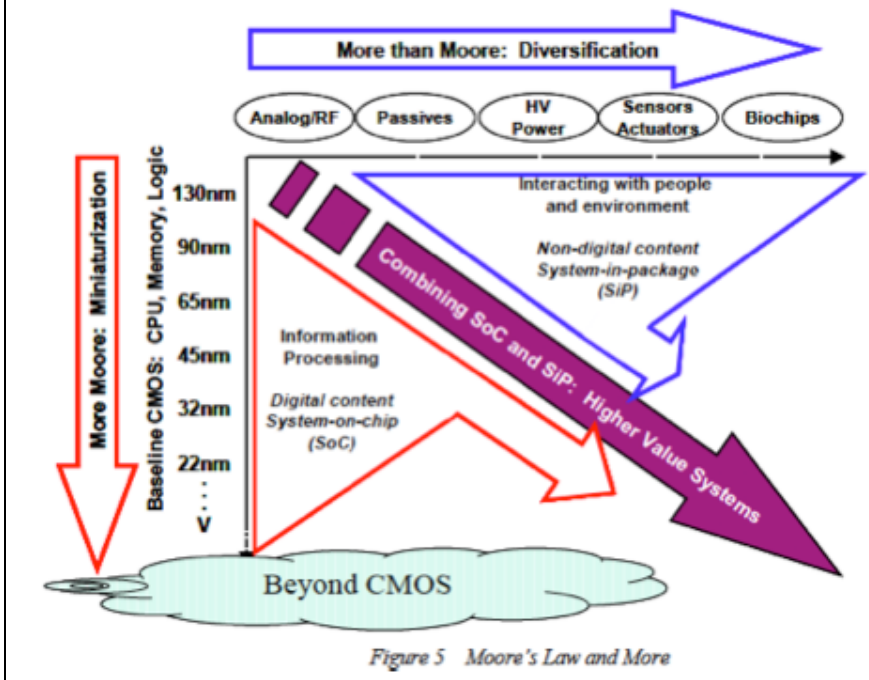

Figure 5 Moore's Law and More

Figure 1: IRDS roadmap pictorial, showing the system trends occurring as CMOS gate length decreases to the smallest achievable. As shown, applications expand to mixed mode systems (like analog/RF, sensor arrays, digital signal processing (DSP), systems on a chip (SoC) and systems in a package (SiP). The cloud entitled "Beyond CMOS" represents the vacuum that must be filled through emerging technology advancements.

As semiconductor industry revenues continue to climb year after year, Moore's law plays out. Moore's law tells us that the number of transistors populating a unit area chip doubles every two years. Driving this trend has been a commensurate technology-driven shrinking of transistor feature size (like gate length, for example). Now, after sixty years of semiconductor technology advancement, achievable transistor feature sizes are leveling out at ~20 nm (~ 40 silicon atoms!) while achievable processor clock rates are saturating at ~10 GB/s. The physical limits of transistor feature size, speed and power dissipation have been anticipated for years. Now it looks like those limits are finally arriving.

IRDS: Each year, technology leaders from the semiconductor industry convene in a non-competitive forum to discuss and update a technology roadmap pointing to the current and future directions of semiconductor technology and markets. The International Roadmap for Devices and Systems (**IRDS**) is that forum. **IRDS** is the modern day successor to **ITRS** (International Technology Roadmap for Semiconductors). It is connected with the IEEE (Institute of Electrical and Electronics Engineers), which plays a major role in standards development for the semiconductor industry.

Figure 1 is a schematic, taken from the IRDS website[1]. It shows pictorially the state of affairs in the semiconductor industry in 2019, as seen by the industry leaders. The abscissa (x-axis) of the graph represents the advent and growth of social media and 5G. Leading the charge to supply the marketplace with interactive, high speed and low power solutions is the technological thrust to develop systems on a chip (SoC) and systems in a package (SiP; that is, multi-chip-modules). The ordinate (y-axis) shows the transistor feature size decreasing to meet performance goals. At the bottom of the figure (gate length less than 20 nm) is a cloud, implying "new breakthrough technology". IRDS calls this cloud **"Beyond CMOS"**.

Superconducting Electronics: There are, as part of IRDS, special working groups tasked to explore a variety of new or novel technologies. New technology candidates include graphene nano-ribbons, carbon nanotubes, molecular electronics, quantum computing *and* superconducting RSFQ logic. These technologies were selected with potential to augment or even replace silicon CMOS. It is noteworthy that superconducting electronics have been included as a potential breakthrough technology in the semiconductor industry.

Potential applications for SC RSFQ logic include processor logic replacement technology), as a stable two-state system in quantum computers, as multi-layer interconnect in ULSI systems on a chip and as ultra-sensitive sensor systems, to name a few.

IRDS has evaluated some embodiments of superconducting electronics, including sensor arrays and especially RSFQ (Rapid Single Flux Quantum) for logic circuits in ULSI platforms[2]. There technology assessments are viewed from an implementation perspective. That is,

1. What are the key performance indicators (KPI) for the technology under consideration?
2. If met, will the KPIs constitute some kind of performance breakthrough in the semiconductor industry?

[1] https://irds.ieee.org
[2] Beyond CMOS 2017

3. What magnitude of effort (manpower, resources, cost) will it take to realize this breakthrough?
4. How long will it take for the technology to establish itself in the marketplace (i.e., roughly what would be the time to break-even)?

These questions are usually not answerable early on in the new technologies lifespan. Only after the KPIs have been verified or modified can they be.

In the case of superconducting electronics, many of the KPIs have been verified. There has been considerable advancement of Rapid Single Flux Quantum logic (RSFQ), primarily by Hypres and Northrup Grumman Inc. Using low temperature superconducting materials like Niobium and Lead, these LTS materials, when operated at liquid Helium temperature (~4K), these companies have implemented high-speed samplers (as high as 20 Gsps) for advanced A-to-D converters along with numerous RF supporting circuits. These components have been used in special high-speed national systems applications.

Out of this work, at least two lessons have been learned.

1. The most important factor in determining performance, power efficiency and reliability is the need to operate these systems at cryogenic temperatures, i.e., <4 K for LTS materials and < 77K for HTS materials like YBCO. The cryo systems have historically been bulky and mechanically complex. Often, they consume more power than any other part of the system and are often the least reliable component in the system.
2. If SC technology is implemented at the IC level, part of the IC must operate at cryo temperature while the rest of the IC must operate at or near room temperature. A new technology of micro (or even nano) cooling must emerge. While such a technology is likely feasible, it will be the "long pole" in implementing SC IC interconnects.

The IRDS roadmap (see Figure 1) recognizes that monolithic integration of dissimilar technologies typically in more complex, with time taken to solve these problems well exceeding more hybrid approaches. To accommodate these realities, the IRDS roadmap includes two classes of solution implementations; namely Systems on a Chip (SoC) and Systems in a Package (SiP). Inclusion of miniaturized cryo systems for integrated superconducting interconnects will likely follow an intense exploratory development path, starting with SiP level development of miniaturized cryo-cooling of a localized superconducting circuits, followed by incremental cooling efficiency and circuit performance improvements. At some point in this process, the monolithic integration of localized cryo-cooling cells in an IC will become feasible and the risks

will be manageable enough to fund the effort. The time period for this process is not at all clear, but it is most likely to be many years.

The localized cryo-cooling challenge is common to all chip-level interconnect scenarios. The challenge is serious but the payoff is substantive. From an intellectual property perspective, the only risks are in patenting too soon in the technologies lifetime.

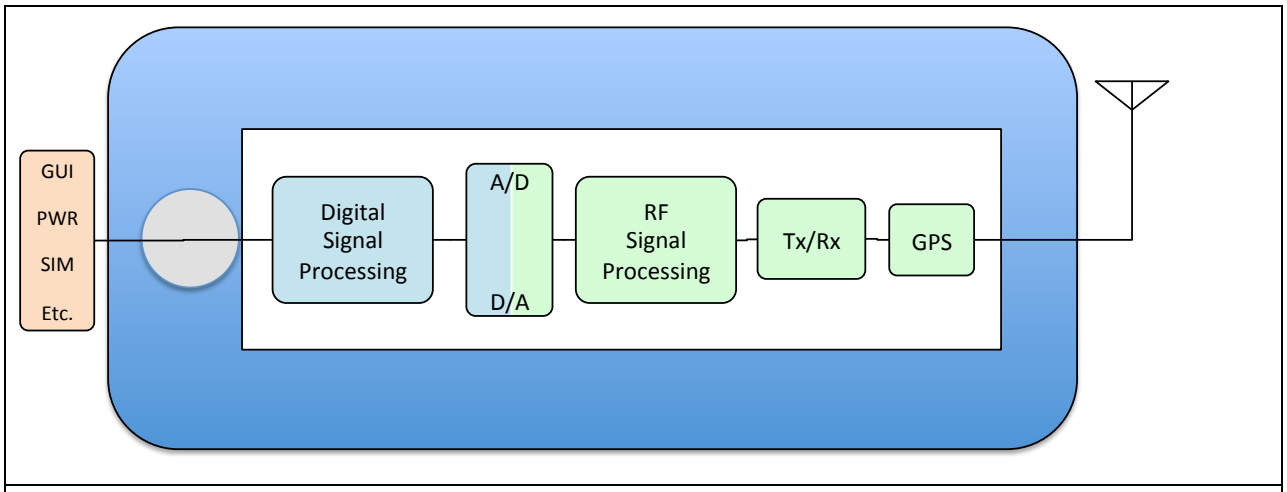

Figure 2: Simplified functional block diagram of the

Cellular Communications Systems

The main driver of the telecommunications markets today is the Fifth Generation wireless technology for digital cellular networks, or 5G. 5G is a set of standards deriving from the next generation cellular radio system architectures. There are three major categories of use case for 5G:

1. **Massive machine-to-machine communications (AKA, "the Internet of Things, or IoT).** Automatic connection of billions of devices without human intervention ("Bluetooth on steroids").
2. **Ultra-reliable low latency communications**
   for interactive real-time control of devices, with signal latency in the ten to twenty milli-second ranges or less.
3. **Enhanced cellular bandwidth (Ultra-Wideband)**
   5G will enable much higher data rates for the user. 5G speeds will range from ~fifty Mbit/s to over two GB/s at the start, growing to as high as 100 Gb/s, at least one hundred times faster than 4G data rates.

For discussion purposes, we separate the wireless communications system into two broad categories, (1) cellular base stations and (2) cell phones. We do this because the physical design requirements for these two categories are different.

Superconductivity in Base Stations

Base stations contain RF and microwave antennas, filter banks, transmitters, receivers, and special digital processing equipment. Functionally, the base station is not unlike file

servers, large switching stations or supercomputers. However, base station environmental factors (like heat and humidity) can be more stringent than in a server or even a supercomputer. In this high performance/high reliability design space, there is often room to pay the price of power consumption to get bandwidth and connectivity in the design. In this large-scale computation environment, power economy is important, but the power scale is very high (up to megawatts) compared to a hand-held Smart-Phone environment where even milli-watts are important. Just as it is in supercomputers, base station designs can benefit from the application of superconductivity because the necessary costs of cryo-cooling (size, weight and power) can be absorbed and isolated in the big picture. Performance breakthroughs (particularly in bandwidth (i.e., clock rate) and latency in some cases can be traded against power consumption and reliability in base station design.

Smart phone environment

Power savings issues in the Smart Phone are very different than in base stations. Smart Phones are battery operated, and as we all know from experience, batteries are limited in their capacity. Power consumption in a Smart Phone is tallied one milli-watt at a time. In this business, the "war on power" is a high-stakes game, often with a winner-take-all outcome.

Here, it is all about silicon ICs operating with power rails at 1.2 volts or even less. The entire power budget for a Smart Phone is typically in the One-Watt range while in use and considerably less in the idle modes. At this time is difficult to justify applications of superconductivity in the Smart Phone physical design environment. The challenges for applying superconductivity to Smart Phones is similar to the issues discussed in the section on superconductivity in the silicon IC industry. The long pole in these design considerations is the need for micro-isolated cryo-cooling elements monolithically integrated with the transistors, interconnect media and RSFQ electronics. This design domain and the intellectual propety that will ultimately be generated will strengthen the value of superconducting electronics, in both semiconductor IC industry and the Smart Phone industry.

As 5G rolls out, the biggest challenge is to continue pulling more performance from silicon ICs while managing the resultant power consumption. Power management in ICs means reducing the total current drain while reducing the voltage in the power rails. High performance ICs expend a large portion of power on high data rate interconnects. Solving these complex issues can happen through clever materials science prior to

implementing solid engineering. The use of a-axis growth strategy in HTS interconnects is an example. Many such solutions are possible when materials science is intelligently integrated with traditional engineering. This solution space is the main thrust of Ambature's strategic system's driven approach to technology development.

Medical Device

Point-of Care Medical Imaging Systems (MRI)

In the original white paper, we described an opportunity for our a-axis growth technology in *Point-of Care Medical Imaging Systems (MRI)*. These units would operate at or around 77K with a very low applied polarizing B field, or perhaps even the absence of a large electro-magnet altogether. We recall from the white paper that with the use of SQUID loop detectors in place of conventional Faraday detectors in the low B-field regime, significant Signal-to-Noise Ratio (SNR) improvement can accrue even though the operation at 77K is less sensitive than LTS operation at 4K.

We further concluded that with the use of HTS rather than low temperature superconducting solutions, the 4K cryo-environment can be altogether eliminated (further reducing size, weight and power), since low B-fields can be produced with ferro-magnets rather than superconducting magnets.

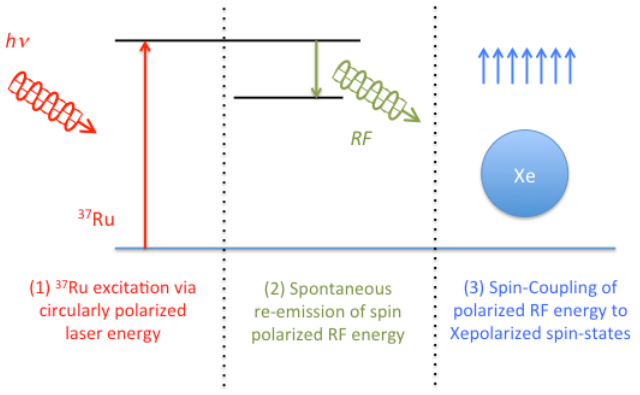

Figure 3: An example of Hyper-polarization technique of enhancing the MRI signal.

There is still has remained a problem (and an opportunity) for point of care MRI architectures. The imaging signal strength derives from nuclear magnetic resonance in the sample and is produced by applying a strong applied magnetic field. When operating in the low field regime, some form of "pre-polarization" is called for to compensate for this loss of signal accompanying the reduced b-fild. In the original use of "pre-polarization", a strong magnetic field is pulsed on for a short time prior to polling the sample at the detector. While the approach produces a sufficient RF signal, it comes at the expense of the size, weight and power consumption that accompanies the electro-magnet; it is sort of like taking a shower in a raincoat. Nevertheless, the industry has pursued this path.

However, there has been progress in the past few years. Innovations have occurred in finding new alternatives to pre-polarize samples without the need for a strong magnetic field. In fact, methods have been devised to pre-polarize samples without any externally applied magnetic field at all. This family of techniques is referred to as "Hyper-polarization".

In one example of Hyper-Polarization, nuclear spin-states are excited via laser or RF energy to invoke "spin coupling" interaction that produces spin polarization in samples that can far exceed the equilibrium states produced by strong applied magnetic fields.

In this example of Hyper-polarization, a three-step process occurs (see Figure 3). First, a sample of Rubidium (^{37}Ru) is illuminated by circularly polarized light from a high power laser (l=0.795 microns). The ^{37}Ru atoms absorb the laser energy and are elevated to a metastable excited state with aligned spins. The laser illumination is strong enough that more ^{37}Ru atoms are excited than would be the case in thermal equilibrium. This step is called optical pumping. In step-two, the atoms spontaneously fall into lower energy states by emitting spin-aligned energy at RF frequencies. In step-three, the spin-aligned RF energy then illuminates the xenon molecules. This interaction is referred to as spin coupling. This illumination, if intense enough, results in spin-state population saturation.

In hyper-polarization, the spin-state configuration is not steady state, as it is with the application of a strong static magnetic field. Instead, the optical pump overpopulates the sample. The result is an NMR signal that is many times stronger than with conventional MRI architectures. The sample can be hyperpolarized by infusing it (through inhalation, ingestion or intravenous injection, for example) and then by imaging.

From the perspective of point-of-care MRI architectures, it is easy to see that the adoption of hyperpolarized MRI constitutes a major shift in the technology. Application of high temperature superconducting SQUID detection with this new sampling modality appears, from a systems perspective, to be an opportunity for lower cost a-axis grown HTS solutions**.**

Summary

To summarize, the semiconductor industry and the cellular communication industry have both been growing in the past several years, to the extent that projections indicate a need for new technologies like HTS to ensure continued growth of these industries. Technology roadmaps like IRDS project strong technology growth to continue. The 5G wireless roadmap and IEEE 5G standards indicate similar growth for the cellular communications industry. These projections all indicate that there is abundant opportunity for superconductive technology in general, and for a-axis grown devices in particular. To illustrate this claim, we have provided a technology update on Hyper-Polarization in point-of-care MRI systems and the application of a-axis grown Josephson Junctions for SQUID loop detectors in the imaging hardware.

Regards,
Davis Hartman
2/11/2020

APPENDIX 1

BEYOND CMOS 2017

4.2.2. SUPERCONDUCTOR ELECTRONICS (SCE)

Superconductor circuits switch magnetic flux using Josephson junctions and store flux in inductors. This is very different from semiconductor circuits, which switch electric charge using transistors and store charge in capacitors. A superconducting loop with inductance *L* and circulating current *I* stores magnetic flux F = *LI*. Unlike a loop made with normal, resistive material, the current can circulate for as long as it stays superconducting. The behavior is analogous to an ideal capacitor, but the loop stores magnetic flux instead of charge.

Only discrete values of magnetic flux are possible in a superconducting loop due to the quantum nature of the superconducting state. A simple description is that the superconducting state is associated with a wave function and that the phase change around a loop must be $2\pi n$, where *n* is the number of flux quanta in the loop. The value of the magnetic flux quantum is F_0 = 2.07 fWb. Expressed in practical units, 1 fWb is equivalent to 1 mA×pH or 1 mV×ps. Phase differences between points within superconductor circuits can be produced by magnetic flux, electric currents, and certain devices. Superconductor phase engineering is an important part of SCE circuit design without analogy in CMOS circuit design.

Single flux quantum (SFQ) digital logic represents digital ‘1’ and ‘0’ by the presence, absence, or location of magnetic flux quanta within a circuit element.

Josephson junctions (JJs) are devices used for switching or their nonlinear behavior. Physically, JJs are 2-terminal devices made like a thin-film capacitor with superconducting plates or contacts. Quantum tunneling of Cooper pairs through the thin barrier layer allows a supercurrent to flow between the contacts with zero voltage drop. The maximum supercurrent is called the critical current, I_C. When the current through a critically damped JJ exceeds the critical current, it switches (the superconducting phase difference across the junction jumps by 2p) and produces a SFQ output. Note that the time-dependent voltages and currents produced by the SFQ output depend on the JJ and circuit characteristics, respectively. The switching energy $E_{SW} \sim I_C F_0$ for Ic = 100 mA, 2×10^{-19} J = 0.2 aJ. Smaller values of critical current I_C are desirable for energy-efficient applications, within limits due to noise and required bit error ratio (BER). For an explanation of simple SFQ gate operation, see Holmes et al.[708]

Current supplied to SCE circuits is used to both compensate for energy dissipated during JJ switching and to shift superconducting phase differences within the circuit, biasing operation in a desired direction. Supply current type (ac or dc) and magnitude depend on the logic family.